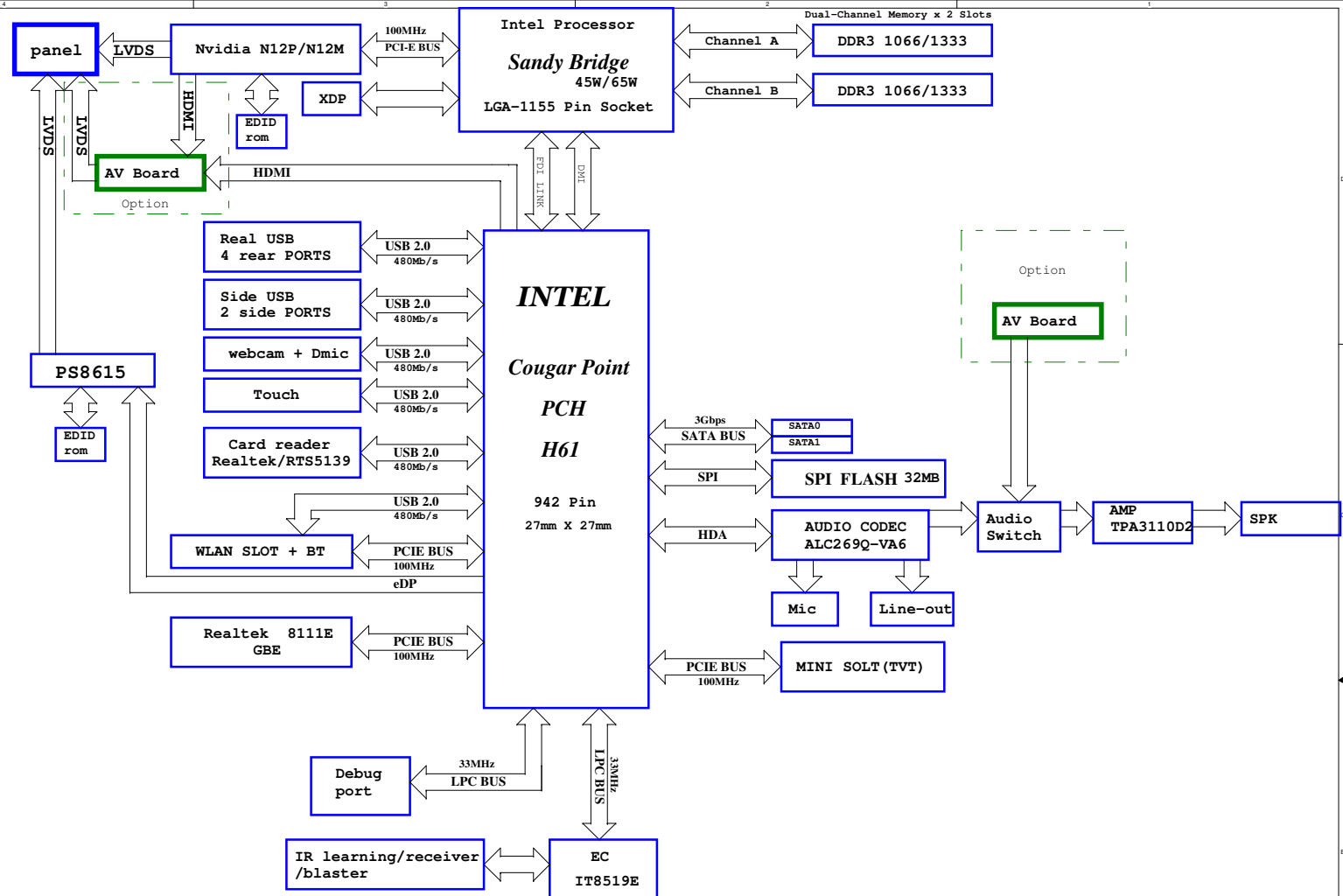
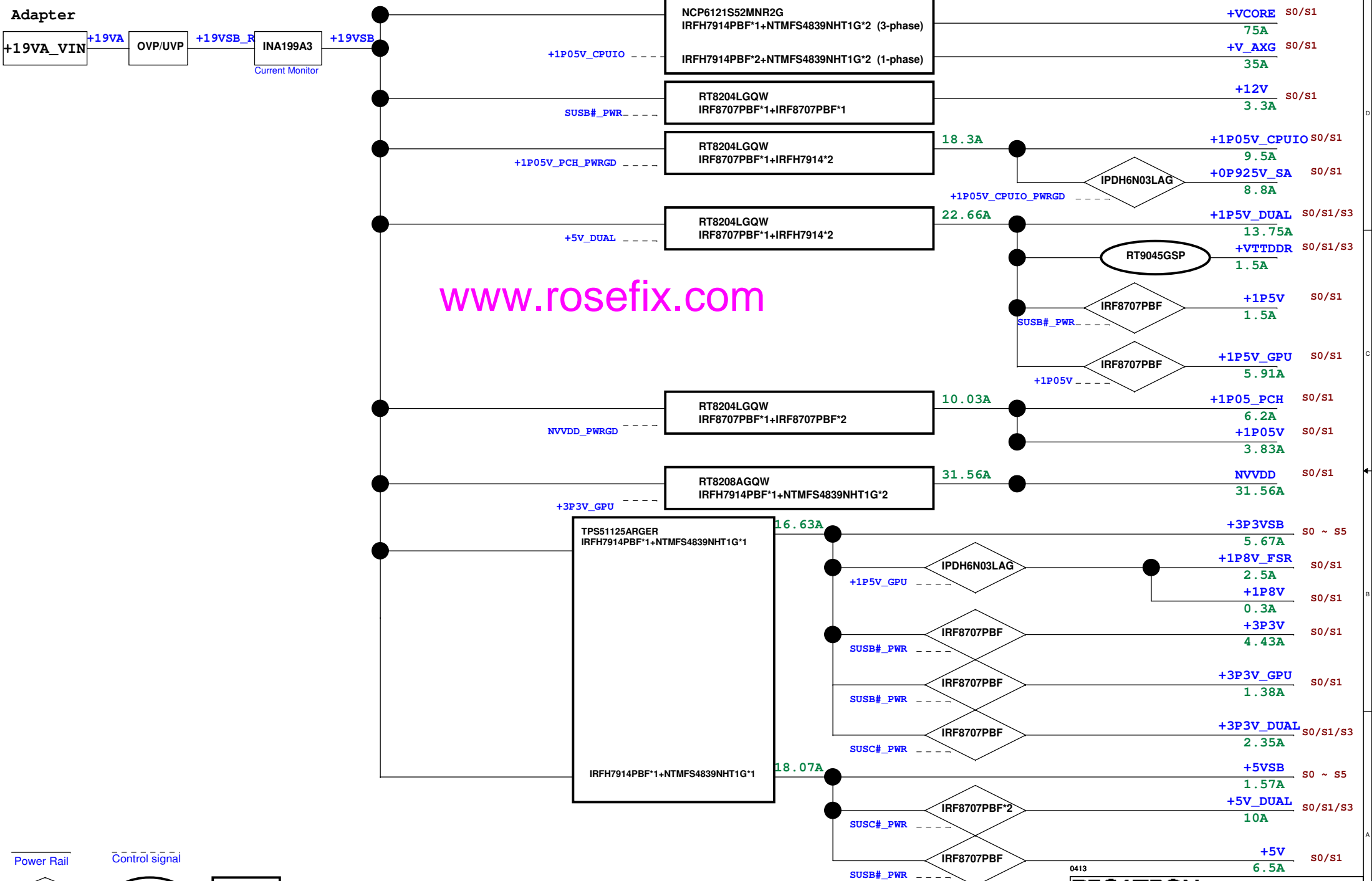


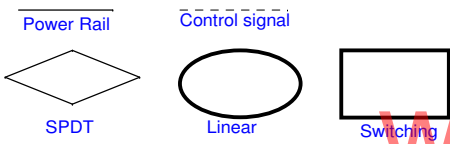
IPPSB-FA

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER FLOW
03	POWER SEQUENCE
04~09	CPU LGA1155 DDR3 A 1-6
10	DDR3 CHANNEL A G/F
11	DDR3 CHANNEL B G/F
12	DDR3 TERMINATION A&B
13	PLTRST CPU# & Smbus
14	Converter Controller
15~16	LVDS&AV CONN
17~25	INTEL PCH 1-9
27~28	LAN
29~30	CODEC&CONN
31~32	AMP&SWITCH
33~35	USB&HUB&BT
36	HPD_DET
37~38	MINI CARD (WL&TVT&DMC)
39	Misc. conn&Touch&Wcam&RTC
40	FAN
41	PWR LED & Button*
42	IR LEDs
43~44	EC 8519
45	SM BUS & SPI ROM
46	SCREW HOLE
47	UVF, OVP & +19VSB
48	LOAD_SWITCH
49	+3P3VSB&+5VSB
50	+1P5V_DUAL & +1P2V
51	Current Monitor
52	+12V & +1P8V
53	+1P05V CPUIO&+0P925V_SA
54	POWER PROTECT
55	+1P05V CPUIO CAP
56	+VTT_DDR
57	+V_AXG DRIVER
58	+VCORE CONTROLLER
59~61	+VCORE CAP
62	+1P05V&+1P05V_PCH
63~64	CPU&PCH XDP DEBUG CONNECTOR
65	VGA CONN
66~67	GPU DDR3
68	VGA-N12P_STRAPPING&EEPROM
69	MXM.VGA-N12P_Xtal/Thermal
70~71	GPU HDMI (DMC&AV)
72	GPU CTRL
73	GPU.VGA_N12P_PCI-E I/F
74	GPU PCI-E LVDS VGA
75	MXM.GPU Discharge
76	GPU POWER&GND
77	MXM.NVDD
78	Card Reader RTS5139-GR
79	EDP CH7511

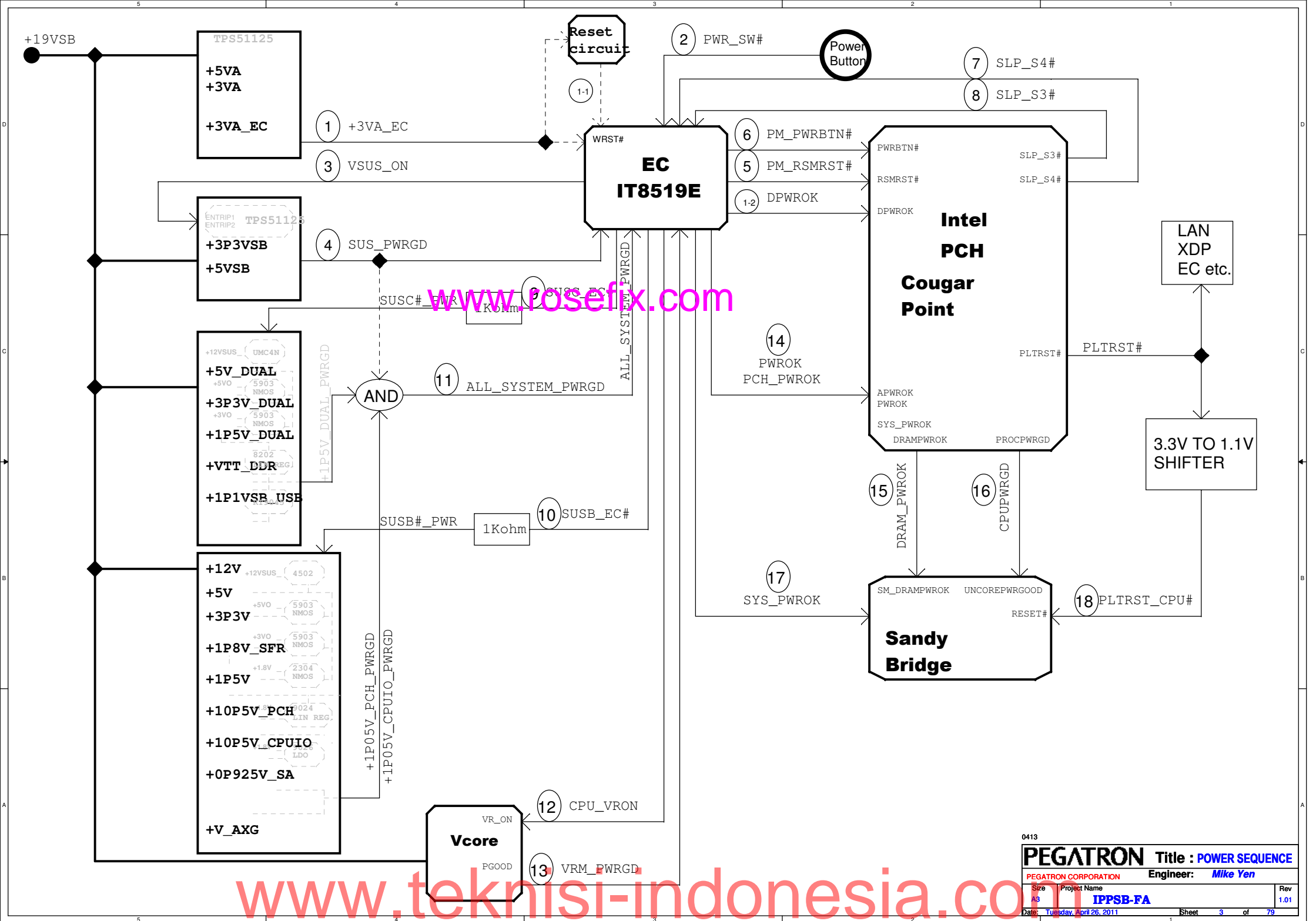


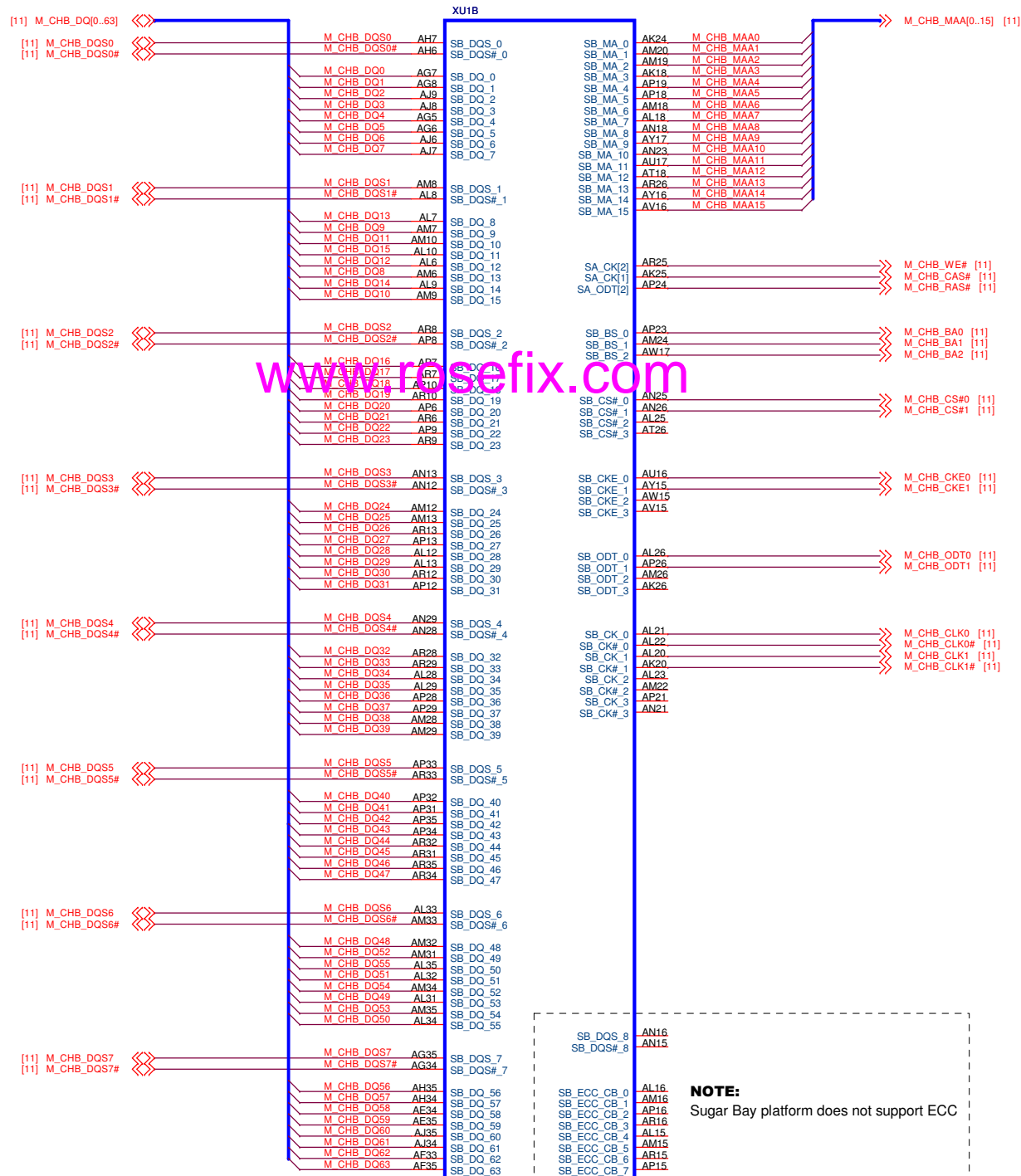


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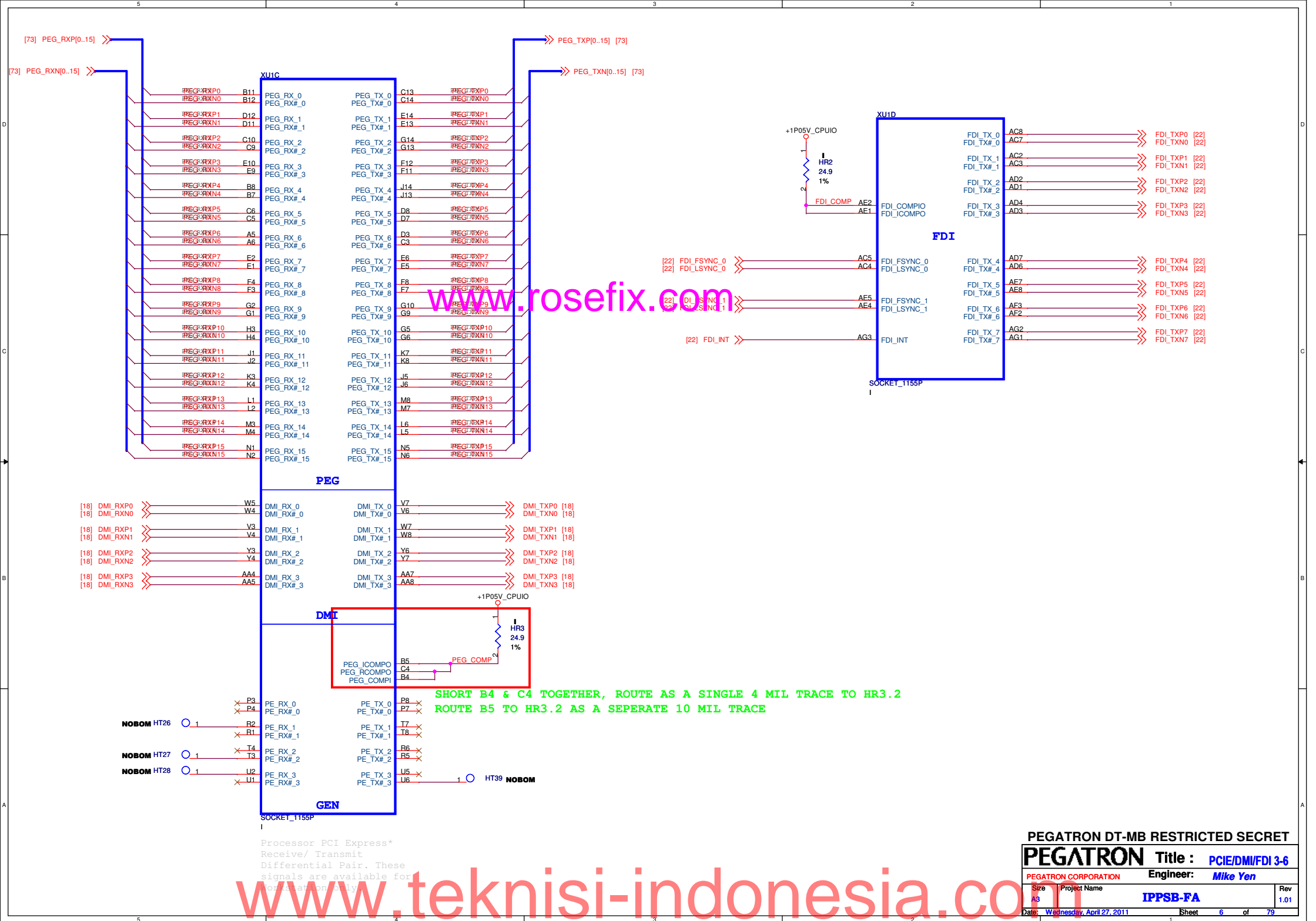
PEGATRON DT-MB RESTRICTED SECRET

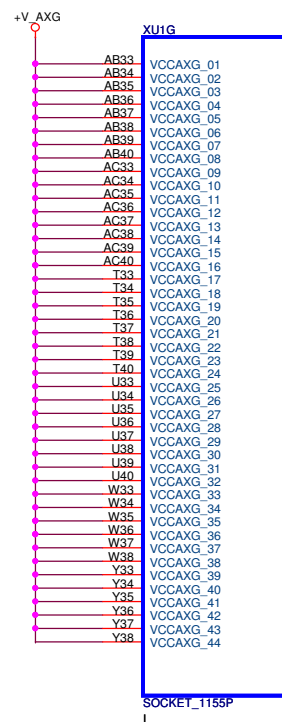
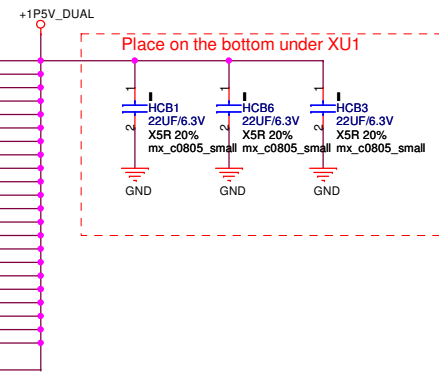
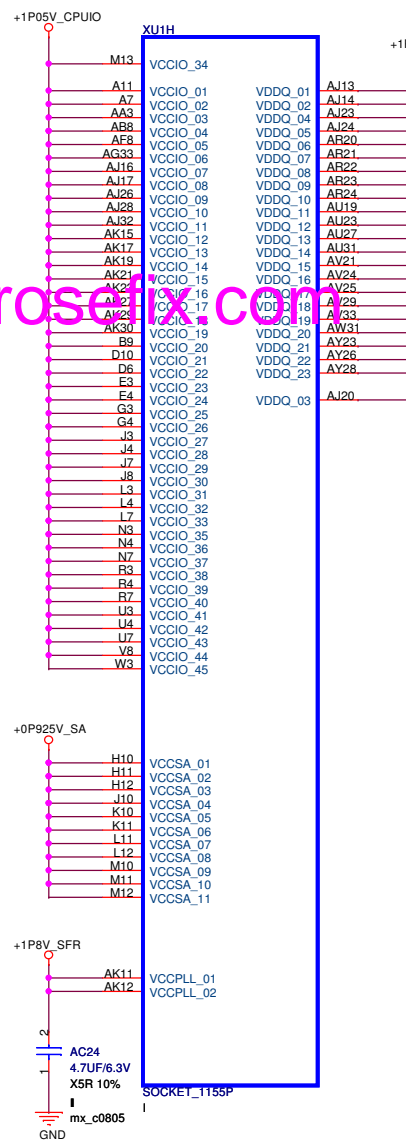
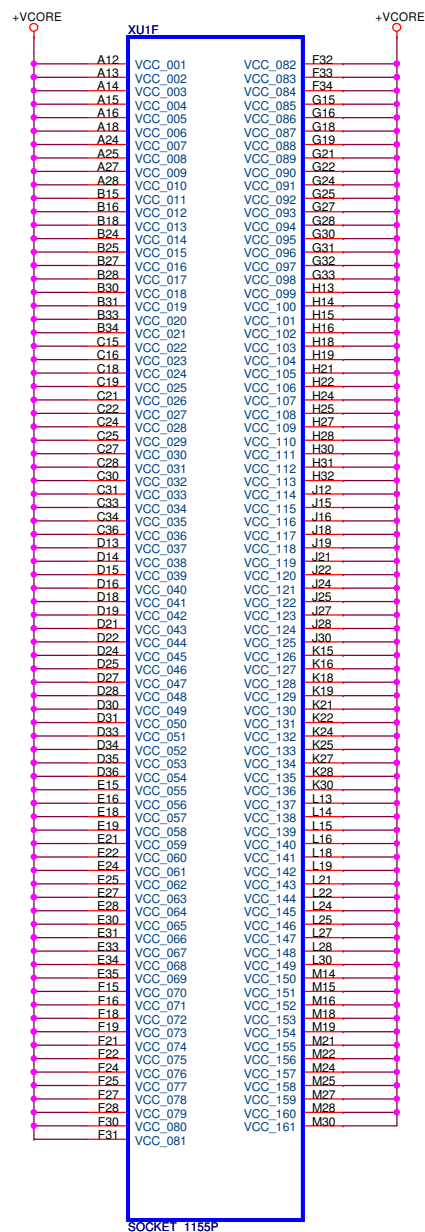
PEGATRON Title : **DDR3 B 2-6**

PEGATRON CORPORATION Engineer: **Mike Yen**

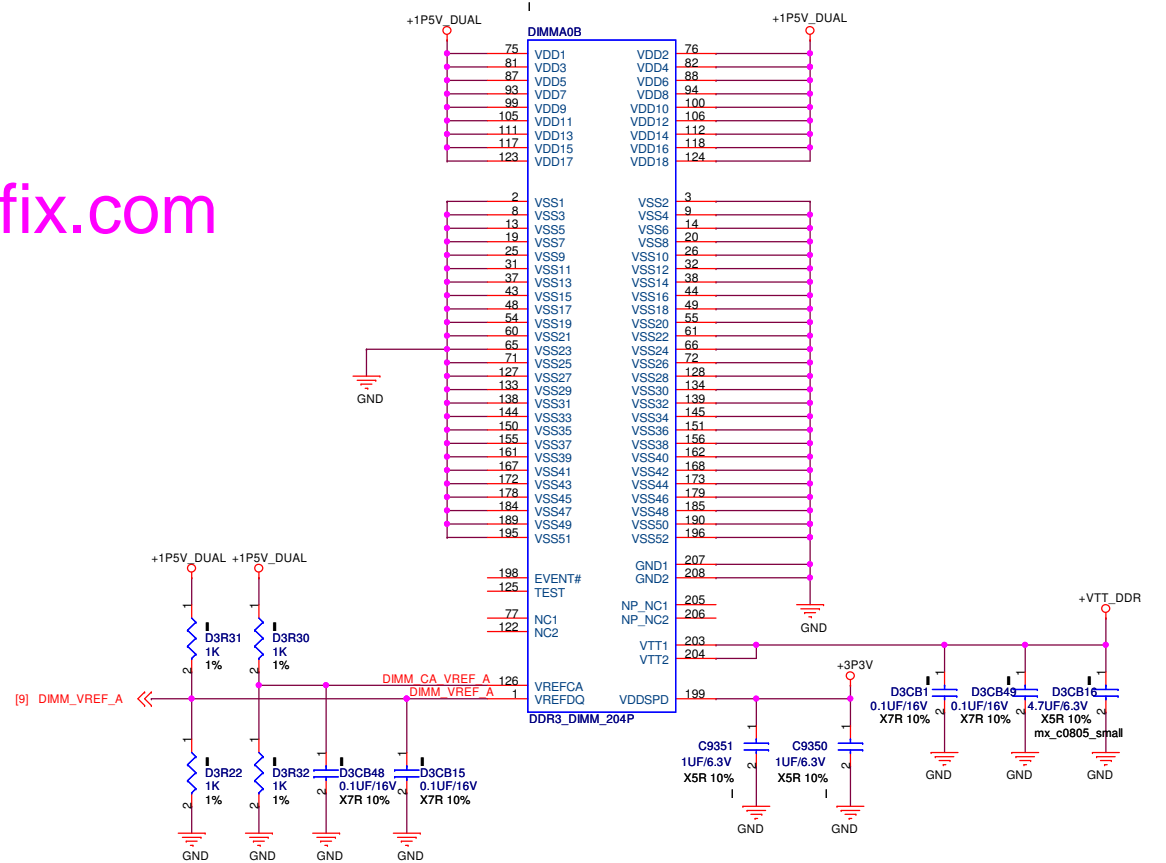
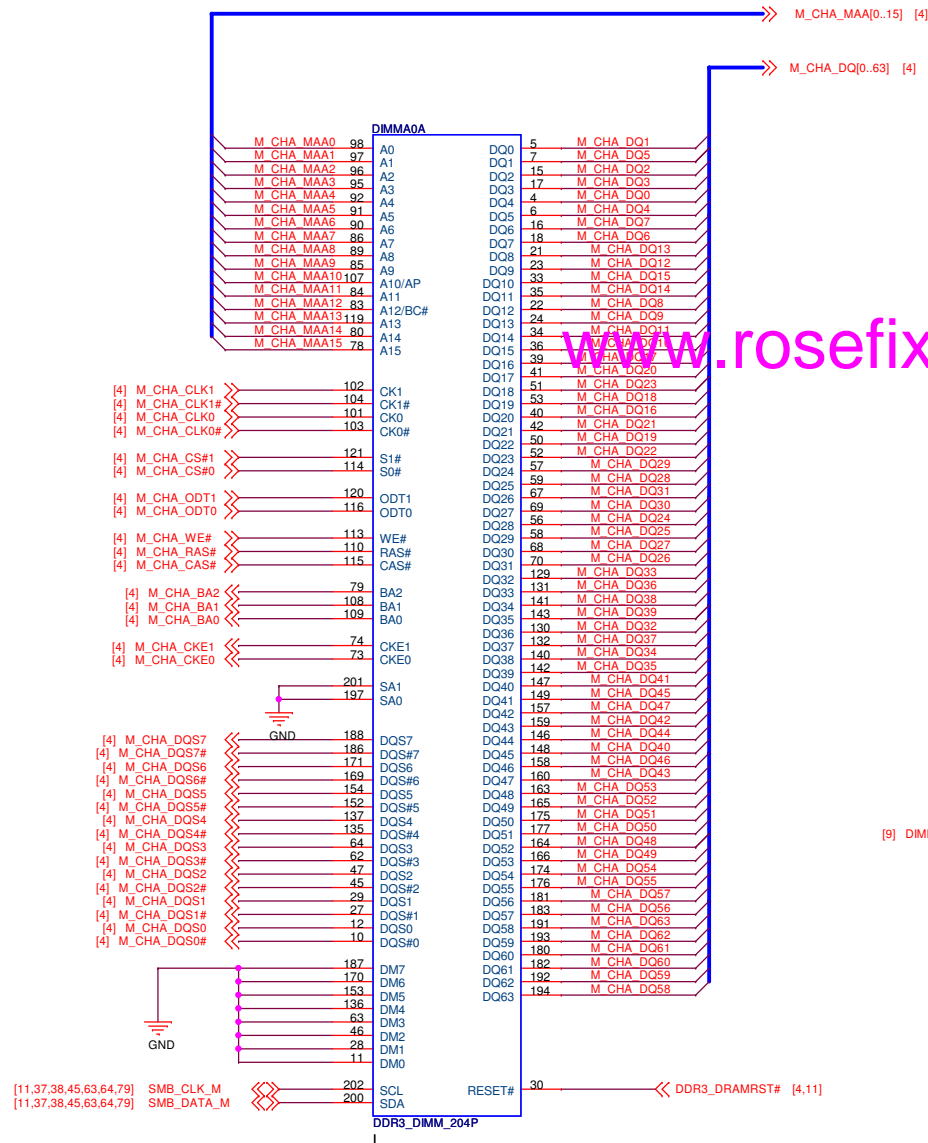
Size A3 Project Name **IPPSB-FA** Rev 1.01

Date: Wednesday, April 27, 2011 Sheet 5 of 79

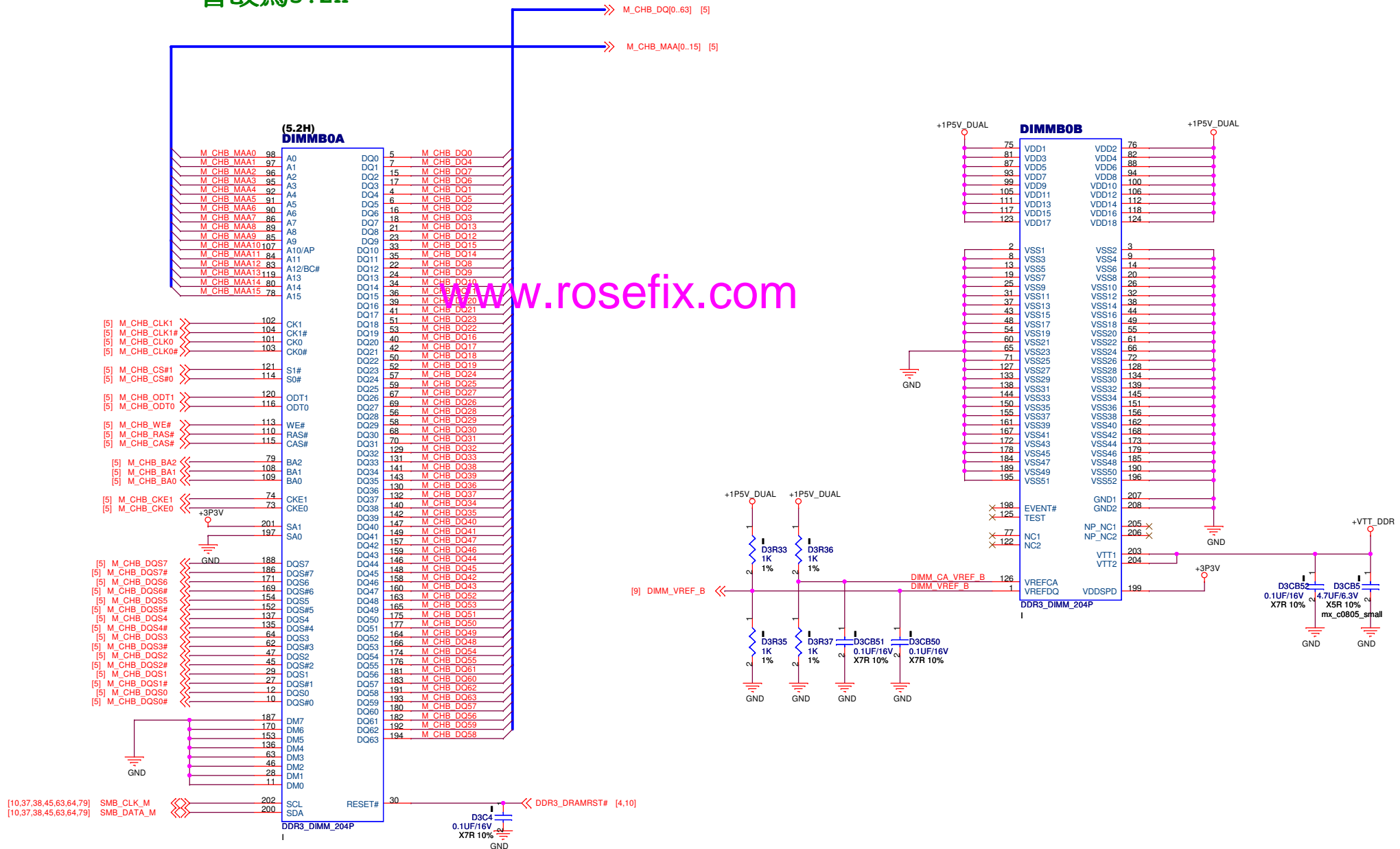


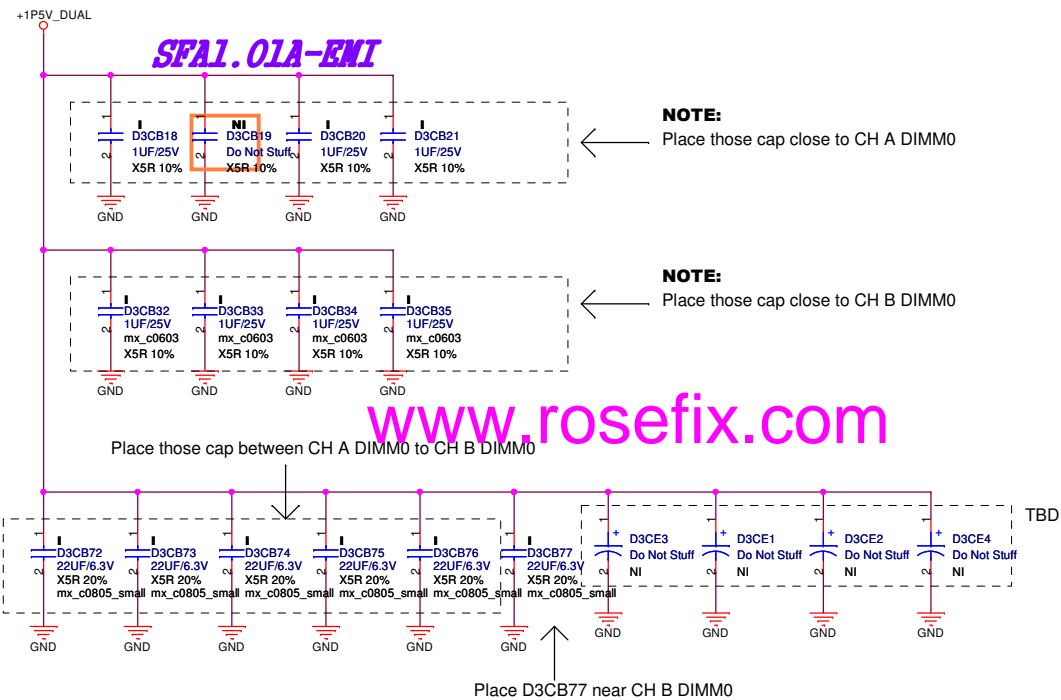


皆改爲5.2H



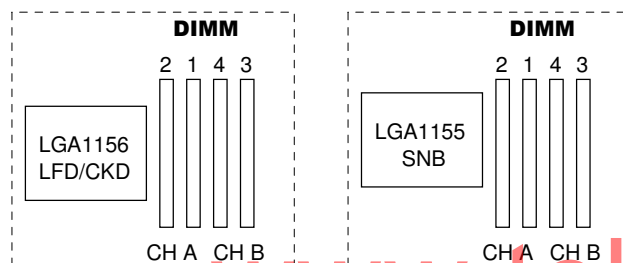
皆改爲5.2H





NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

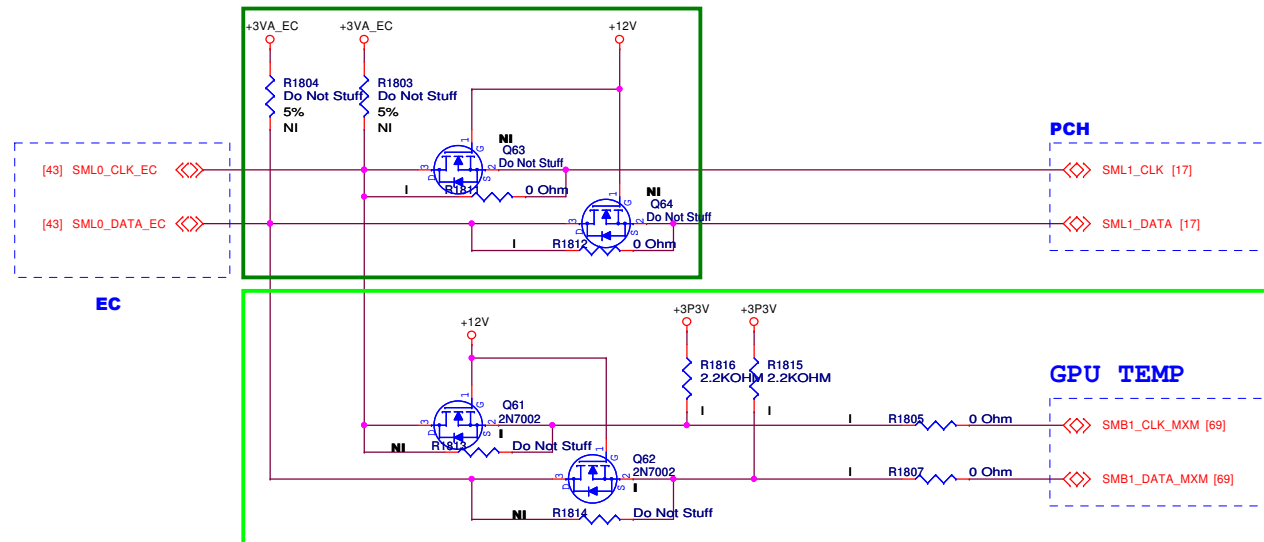
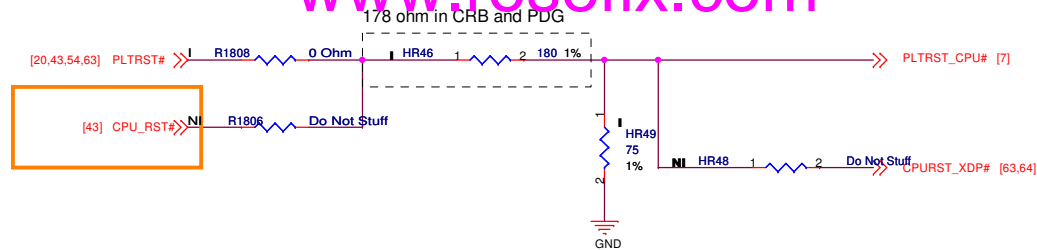
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 12 of 79

PLTRST_CPU#

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PEGATRON DT-MB RESTRICTED SECRET

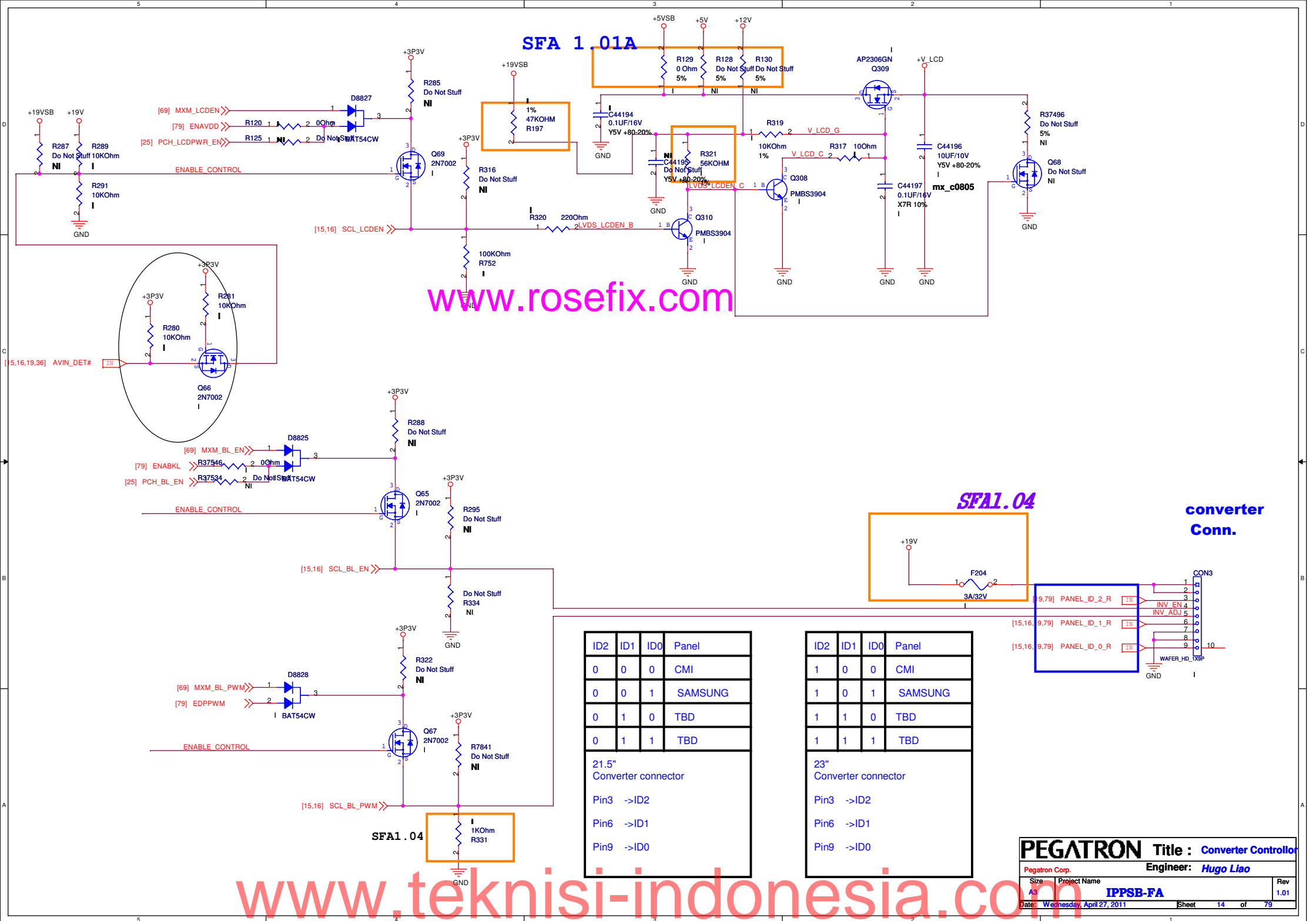
PEGATRON Title : PLTRST_CPU#&SMBus

PEGATRON CORPORATION Engineer: XXXX-XX

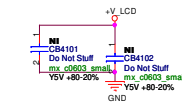
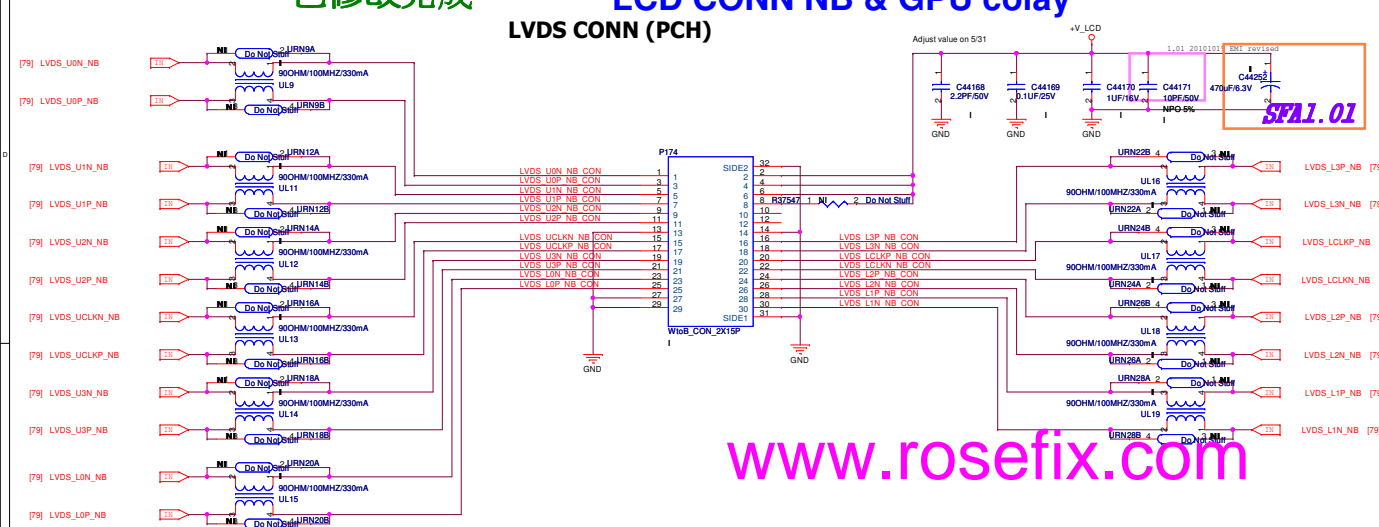
Size Project Name IPPSB-FA Rev 1.01

Date: Wednesday, April 27, 2011 Sheet 13 of 79

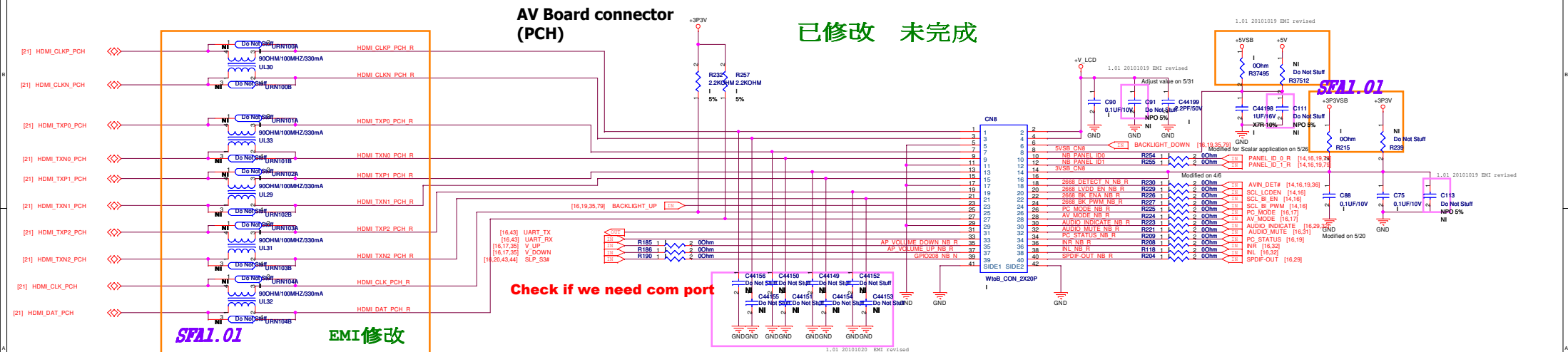
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LCD CONN NB & GPU colay



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LVDS CONN (GPU)



AV Board connector (GPU)

Check if we need com port

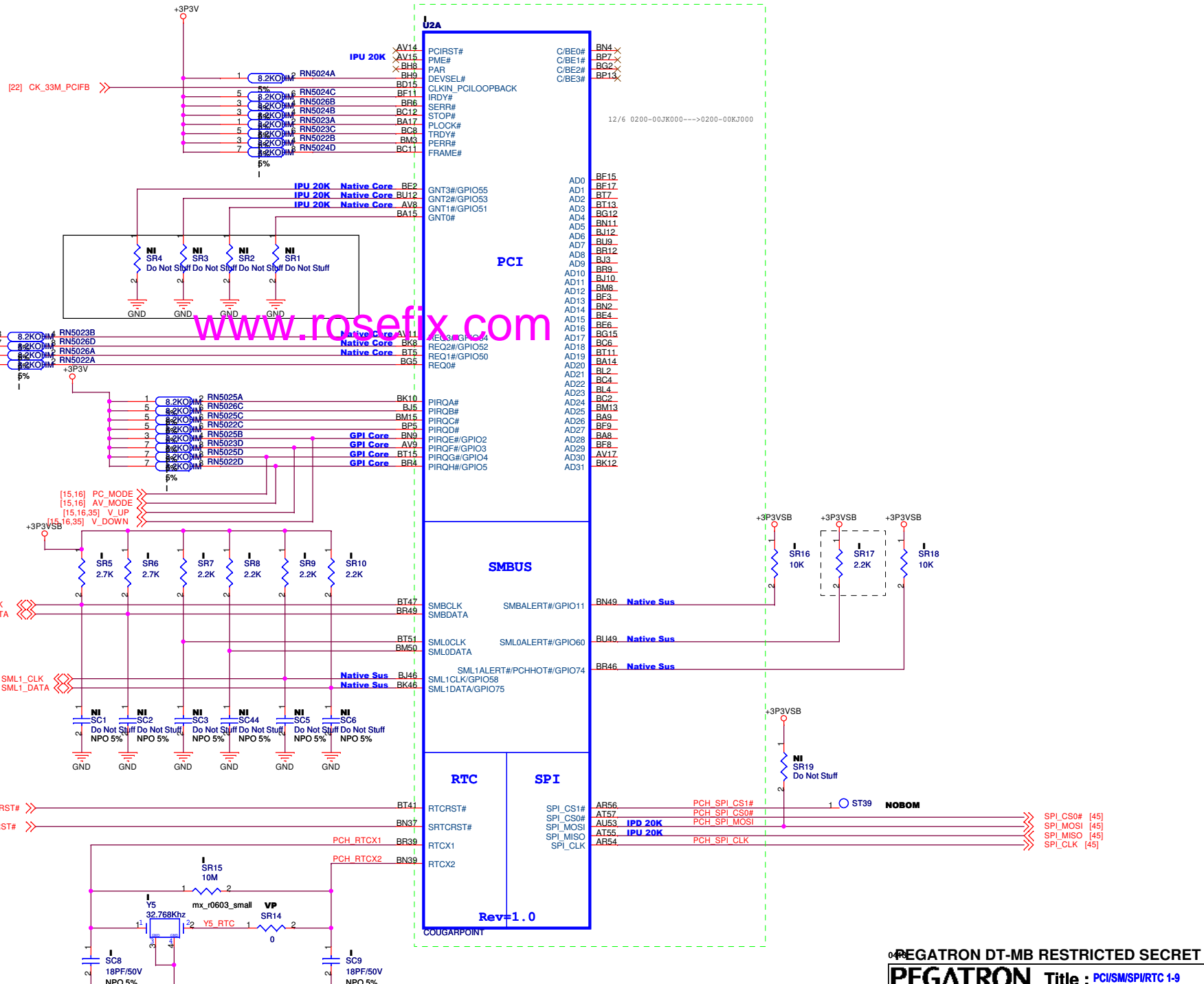


PEGATRON		Title : LVDS CON
PEGATRON CORPORATION		Engineer: Mike Yen
Size	Project Name	R
A2	IPPSB-FA	1.

NOTE: Strapping Options Flash

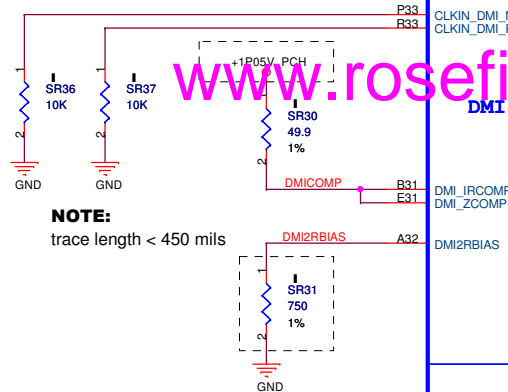
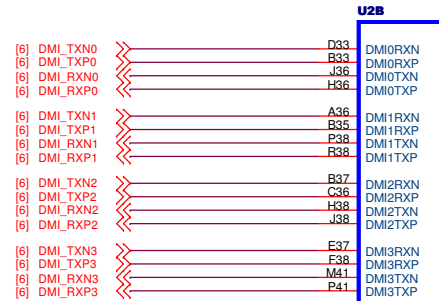
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3
for accelerometer



NOTE:

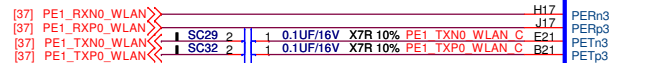
Used for for DMI, PCIe(PCle 2.0 jitter spec compliant).



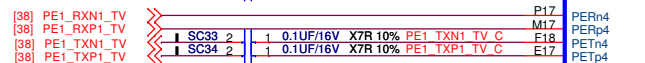
NOTE:

trace length < 450 mils

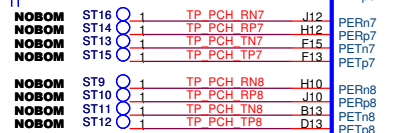
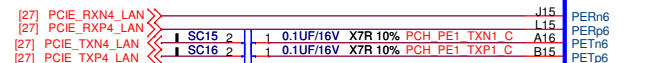
WLAN



TVT

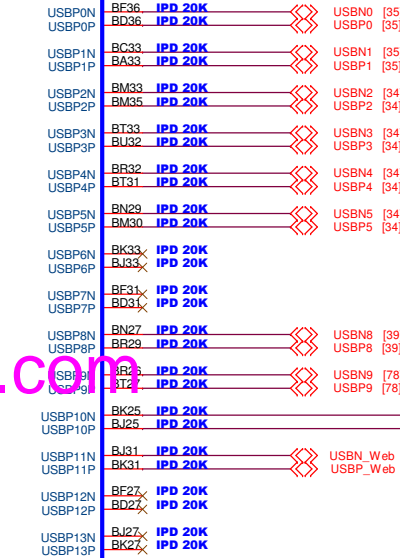


LAN



for H61,
PCIe ports 7 and 8 are disabled.

U2B



side x2 #1 USB Debug port

Rear x4

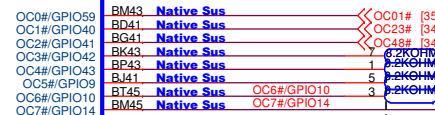
Touch Panel

CARD READER

#9 USB Debug port

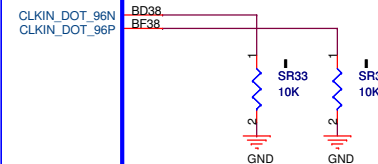
Web Cam

USB



NOTE:

Used for integrated graphics, generate USB backbone,
24MHz HDA bit, and 48MHz clock.



NOTE:

trace length < 200 mils

COUGARPOINT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/USB/DMI 2-9

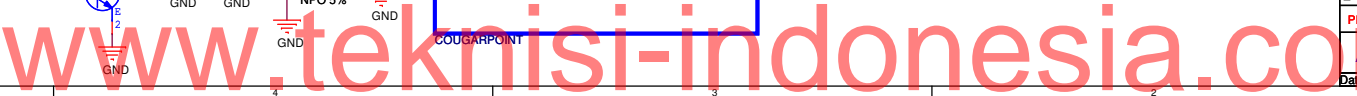
PEGATRON CORPORATION Engineer: Mike Yen

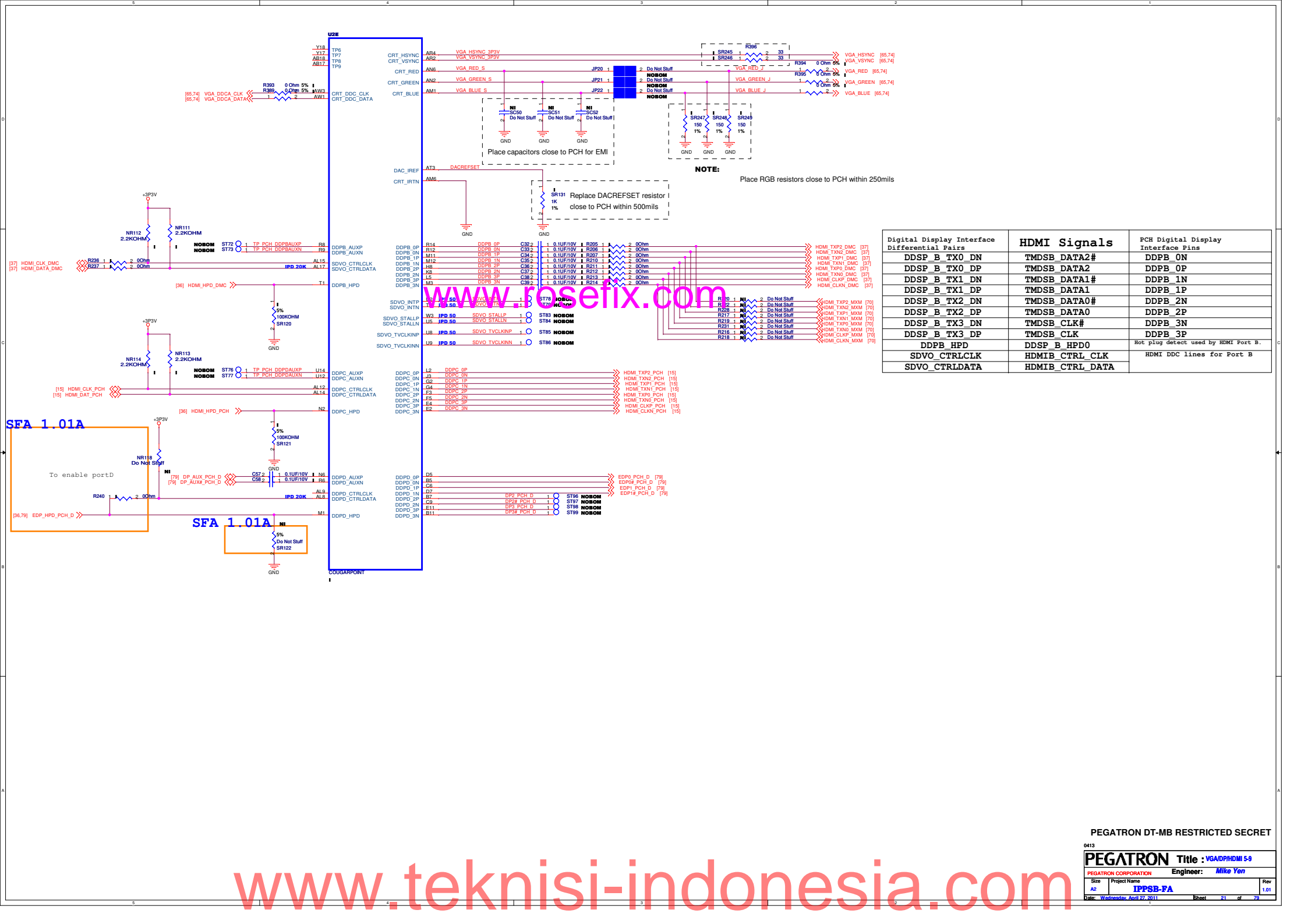
Size Project Name

A3 IPPSB-FA

Date: Wednesday, April 27, 2011 Sheet 18 of 79

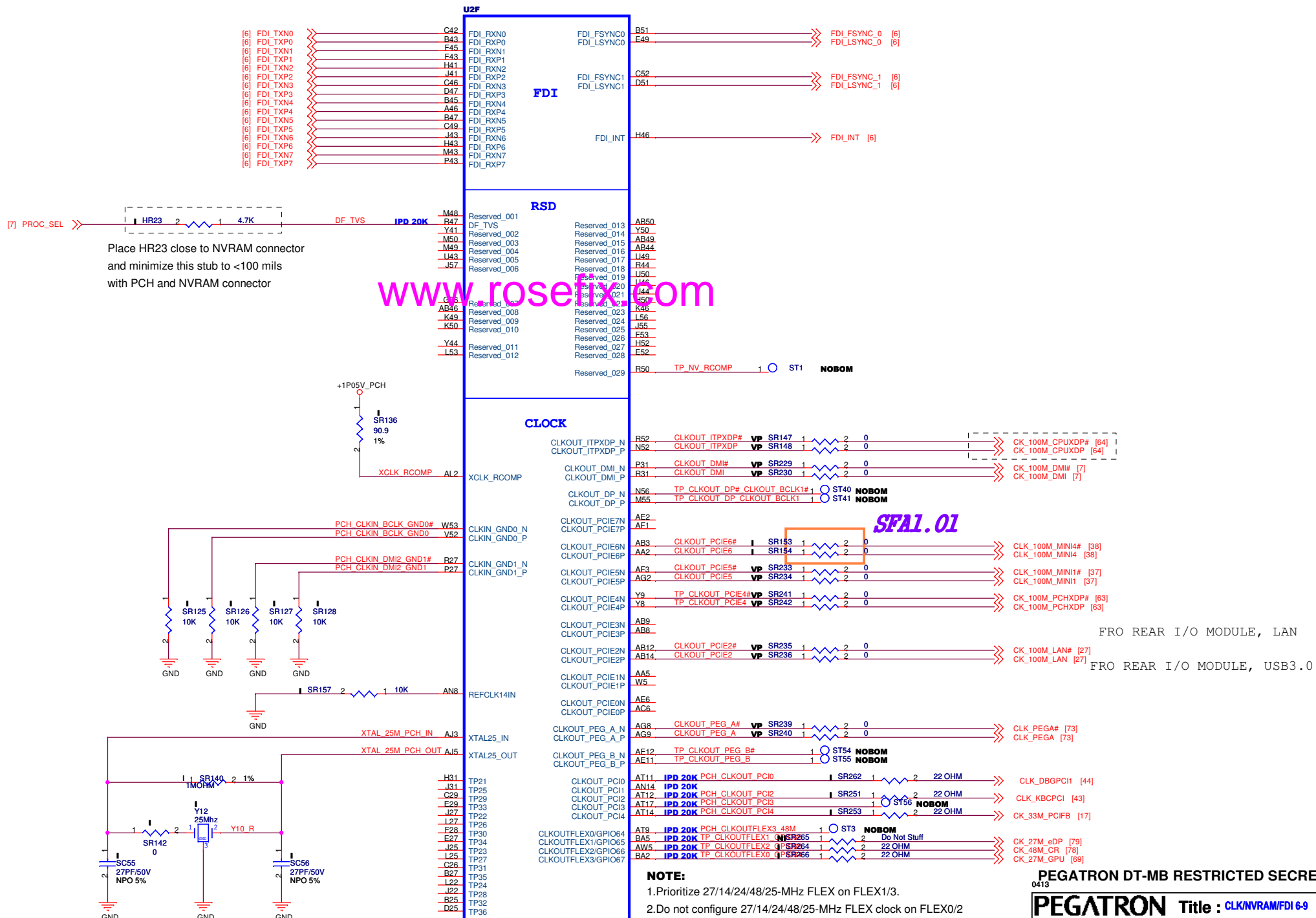
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Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIB_CTRL_DATA	

PEGATRON DT-MB RESTRICTED SECRET



Place HR23 close to NVRAM connector and minimize this stub to <100 mils with PCH and NVRAM connector

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SFA1.01

FRO REAR I/O MODULE, LAN

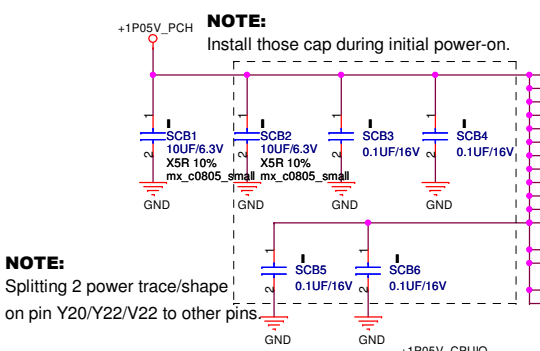
FRO REAR I/O MODULE, USB3.0

NOTE:

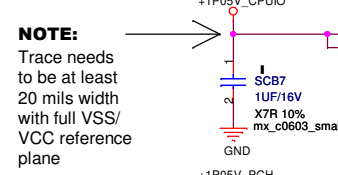
1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

PEGATRON DT-MB RESTRICTED SECRET

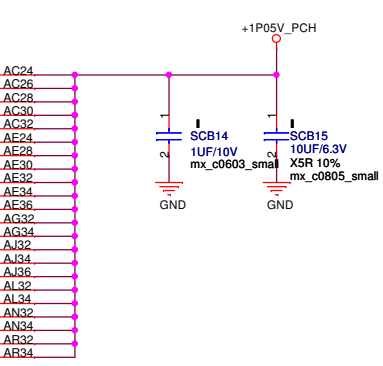
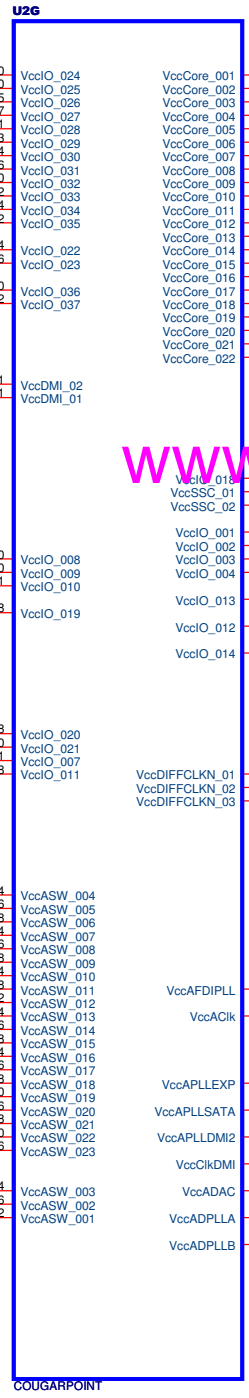
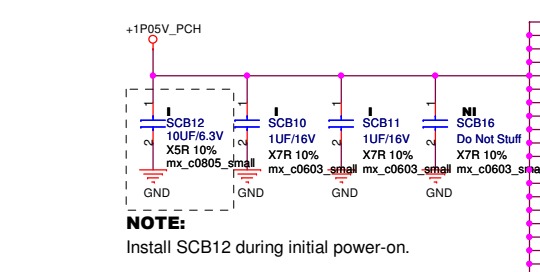
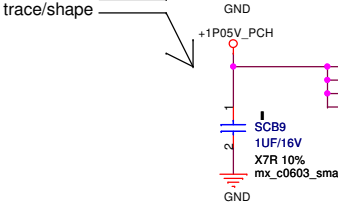
PEGATRON		Title : CLK/INVRAM/FDI 6-9	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name	IPPSB-FA	
Date: Wednesday, April 27, 2011	Sheet 22	of 79	



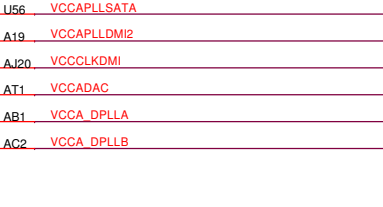
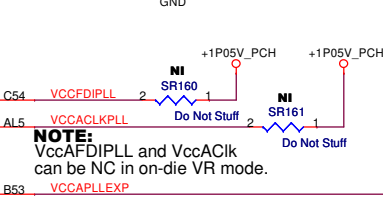
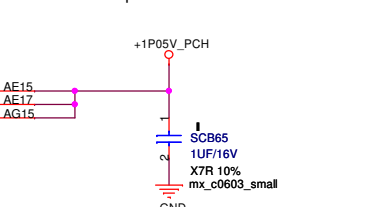
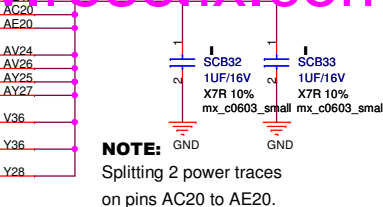
NOTE:
Splitting 2 power trace/shape on pin Y20/Y22/V22 to other pins.



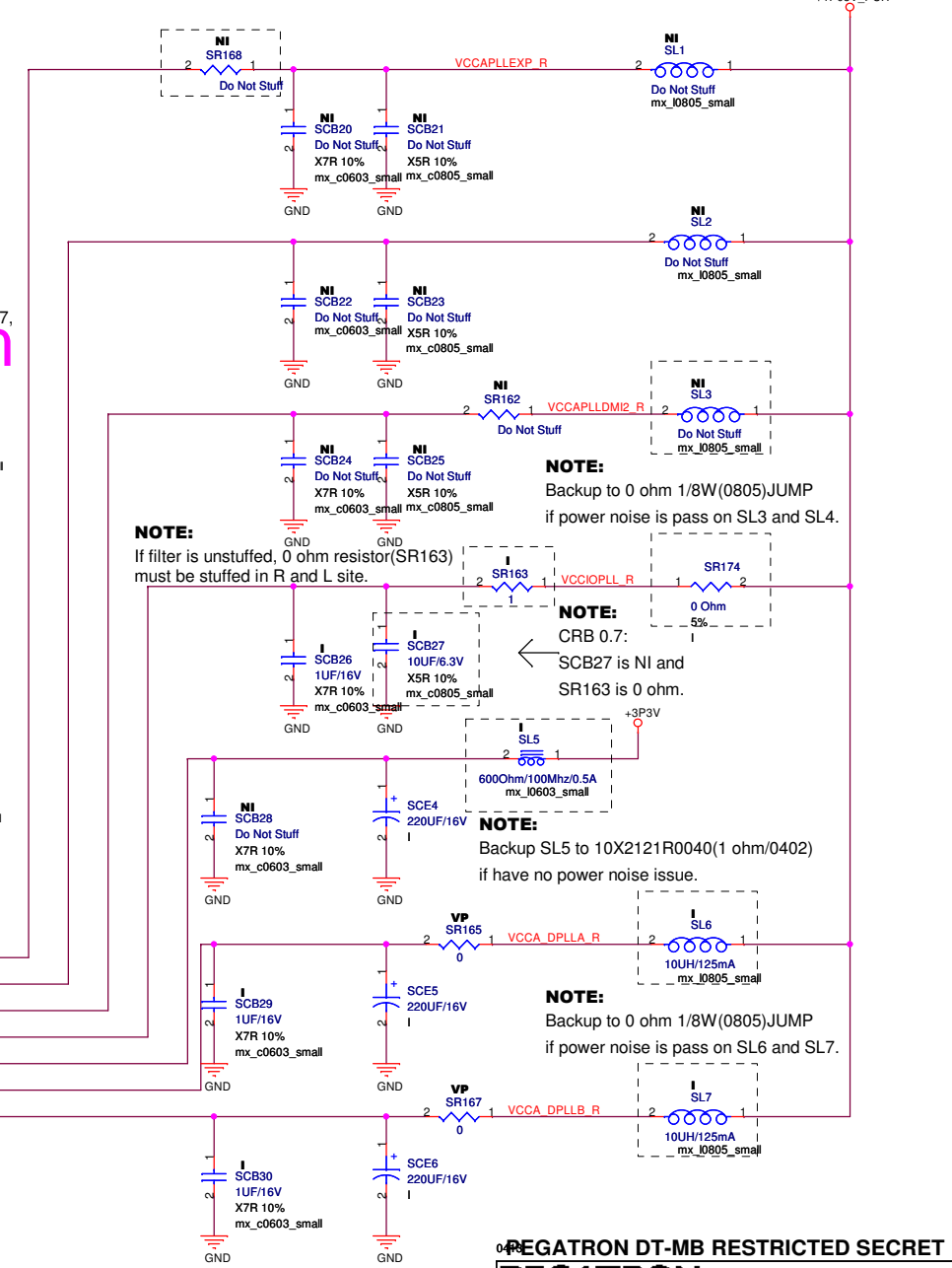
NOTE:
Splitting 2 power trace/shape



NOTE:
Splitting 2 power trace/shape on pins AV24/AV26 to AY25/AY27, and AV41 to AG31/AG40.



NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC in On-Die VR mode.



NOTE:
Place SCB59 and SCB66 near pin AU20,
SCB60 near pin AL38,
SCB61 and SCB67 near BC17.

NOTE:
Splitting 2 power trace/shape on
pin AV20/AU20 and AU22.

NOTE:
Install SCB58 during initial power-on.

NOTE:
Install SCB31 during initial power-on.

NOTE:
Splitting 2 power trace/shape on
pin AV28, AY31/AY33, and AV30/AV32.

NOTE:
Place SCB53 near pin BT35, SCB54 near pin U31,
and SCB69 near pin AV30/AT40.

NOTE:
Place SCB56 near PCH within 40mils.

NOTE:
Just for measurement.

CRB 0.7 is 1uF

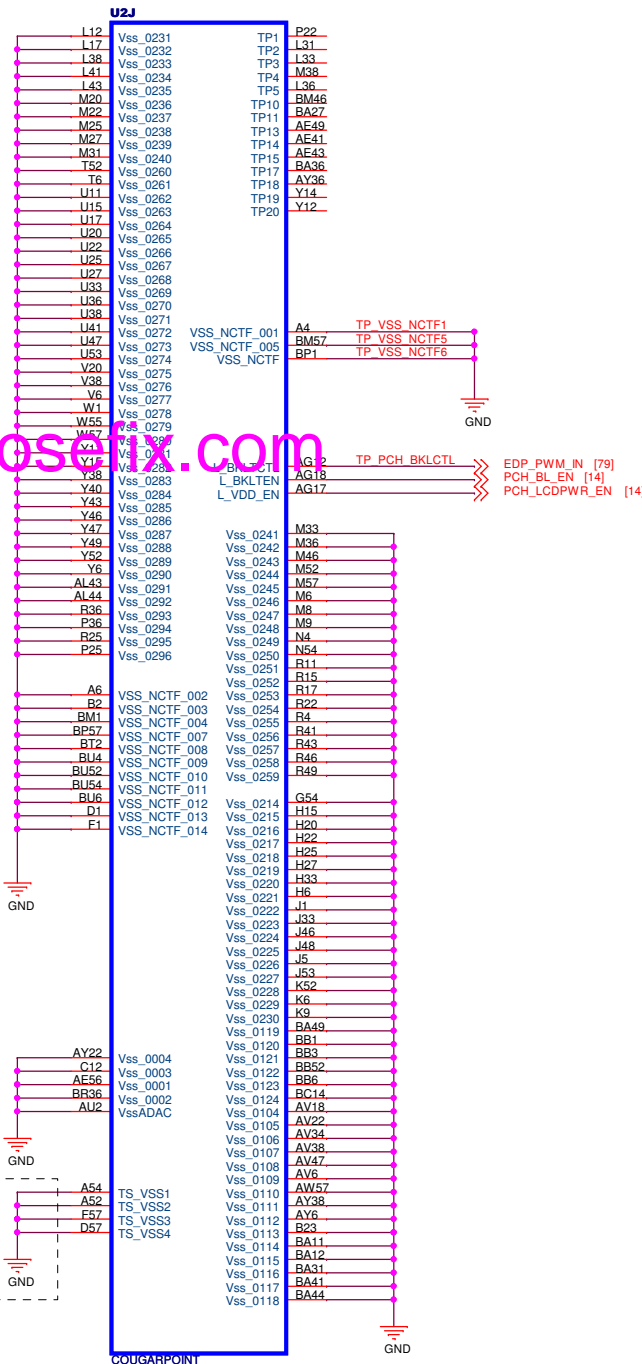
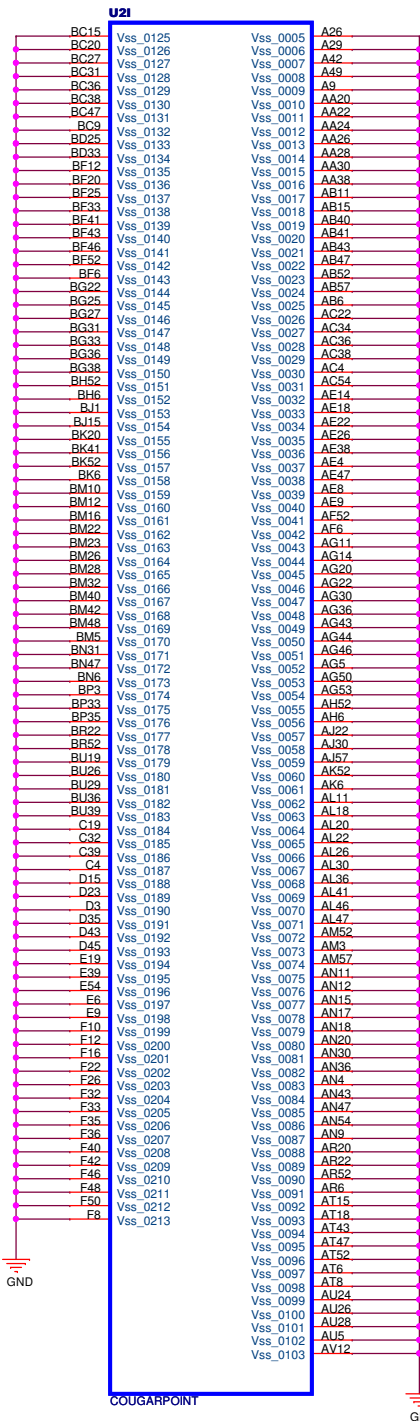
COUGARPOINT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCCSUS 8-9
PEGATRON CORPORATION Engineer: Mike Yen

Size	Project Name	Rev
A3	IPPSB-FA	1.01
Date: Tuesday, April 26, 2011	Sheet 24 of 79	

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NOTE:
BOM option depend on thermal result

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 9-9

PEGATRON CORPORATION Engineer: Mike Yen

Size Project Name A3 IPPSB-FA

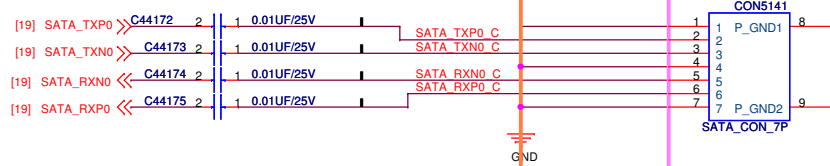
Date: Wednesday, April 27, 2011 Sheet 25 of 79

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已更改完成

SATA HDD CON

1.01 20101019 revised



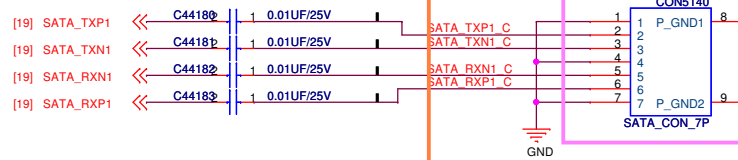
SATA CONTROLLER #1
(MASTER)

COLOR = DARK BLUE

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SATA ODD CON

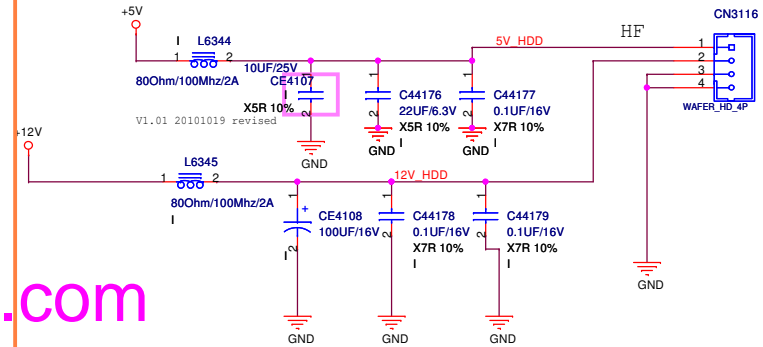
1.01 20101019 revised



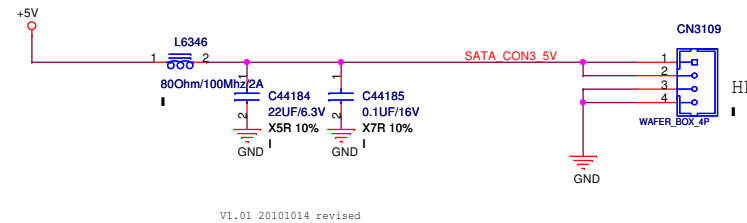
SATA CONTROLLER #2
(SLAVE)

COLOR = WHITE

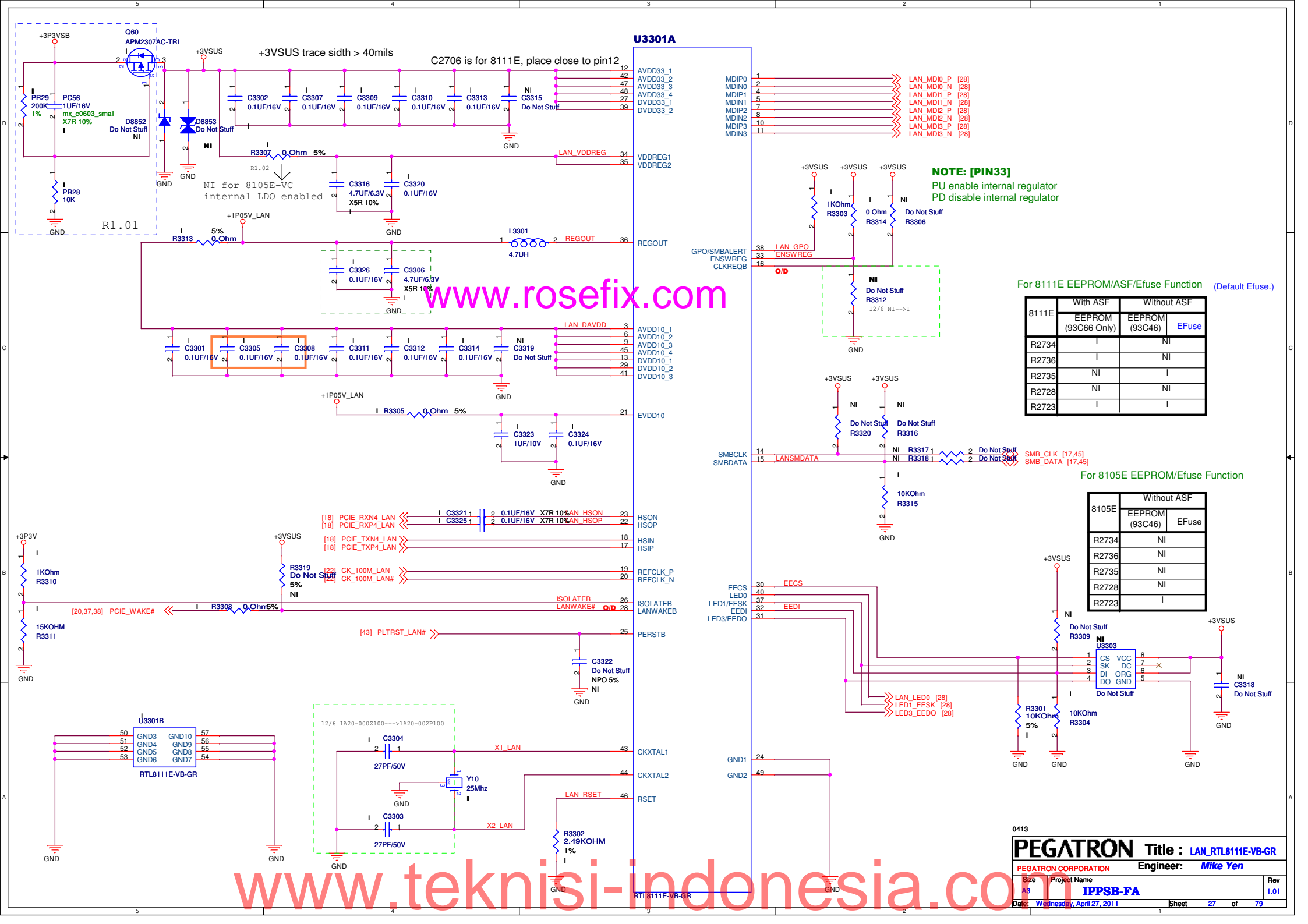
SATA POWER CONN.



ODD POWER CONN.



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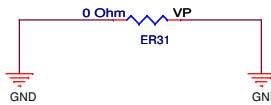
For 8111E EEPROM/ASF/Efuse Function (Default Efuse.)

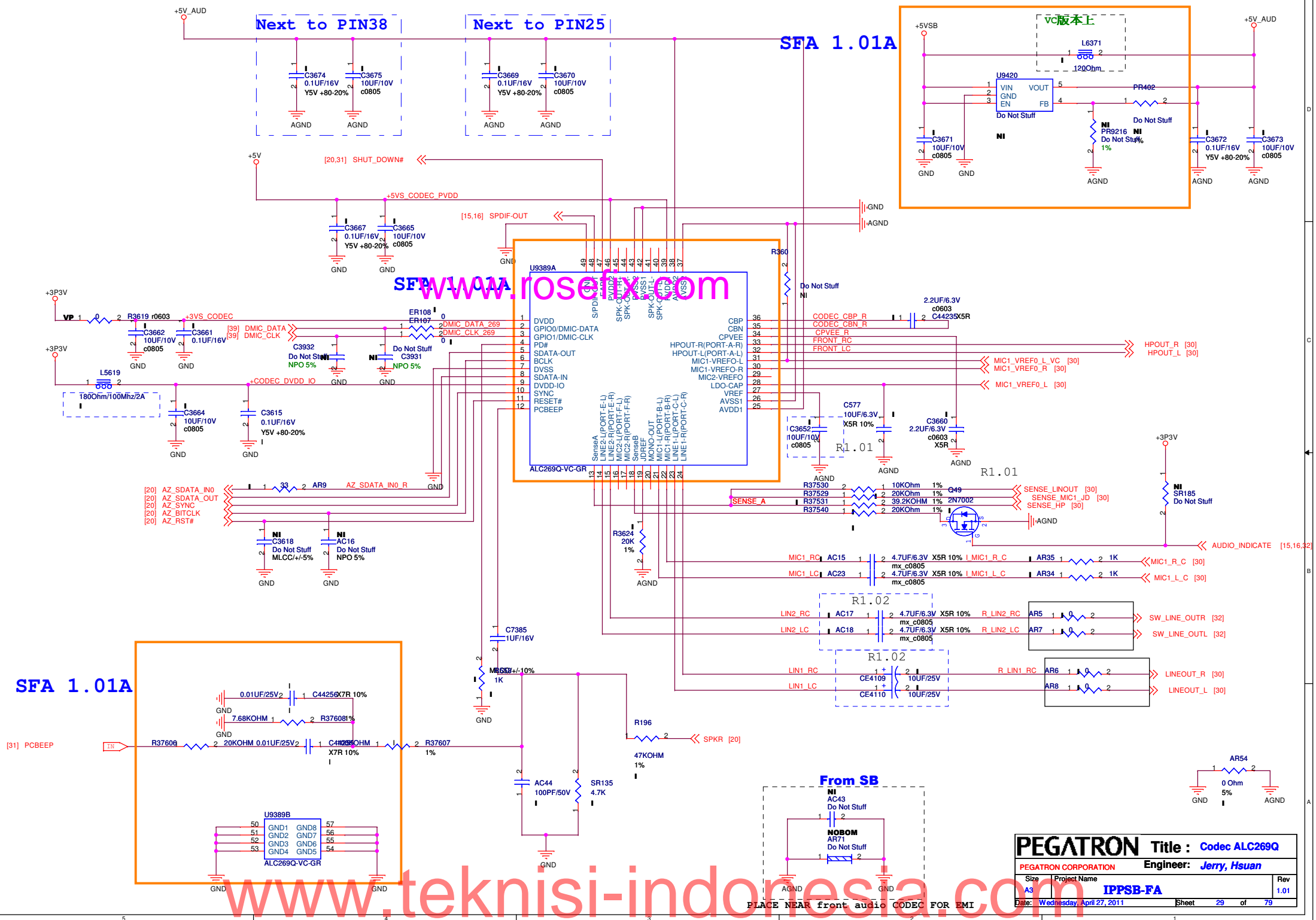
8111E	With ASF	Without ASF
	EEPROM (93C66 Only)	EEPROM (93C46) EFuse
R2734	I	NI
R2736	I	NI
R2735	NI	I
R2728	NI	NI
R2723	I	I

For 8105E EEPROM/Efuse Function

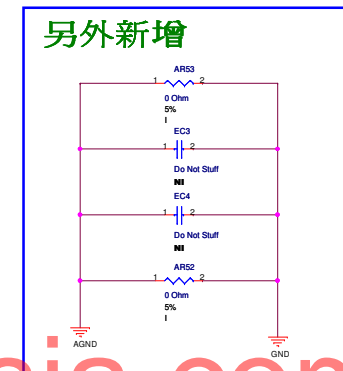
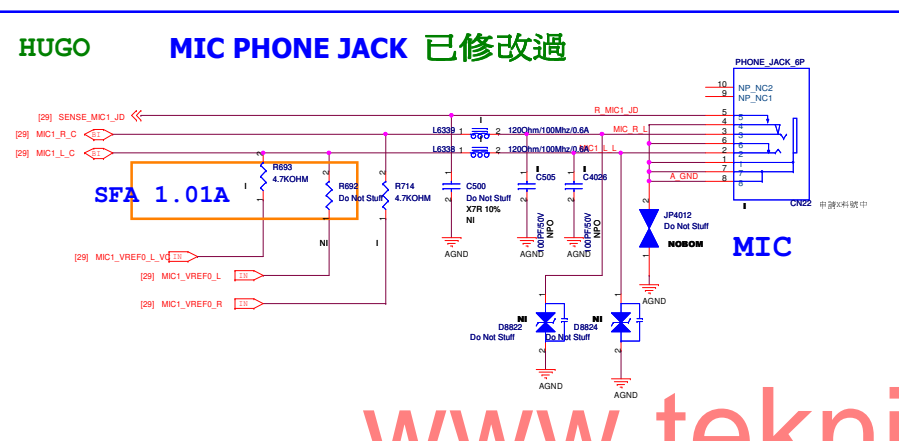
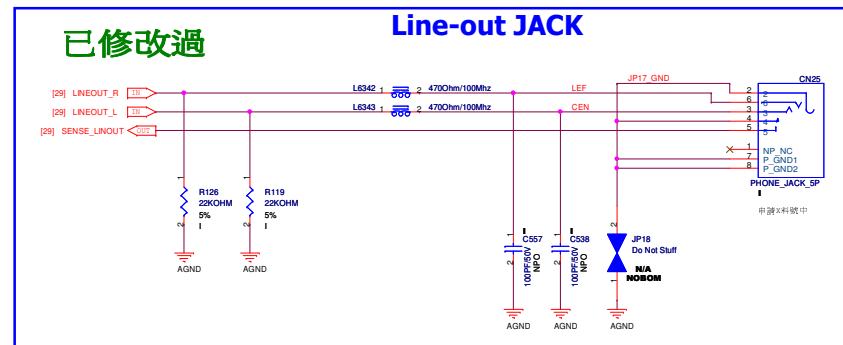
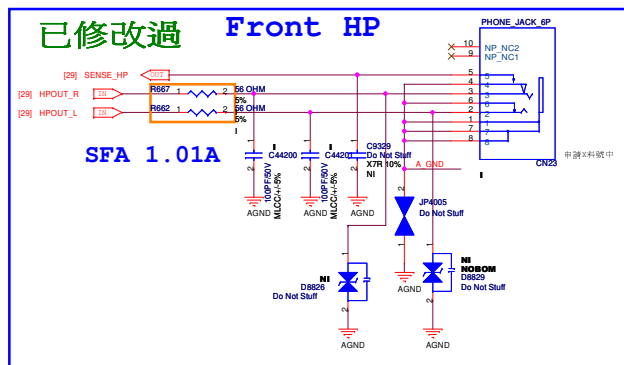
8105E	Without ASF
	EEPROM (93C46) EFuse
R2734	NI
R2736	NI
R2735	NI
R2728	NI
R2723	I

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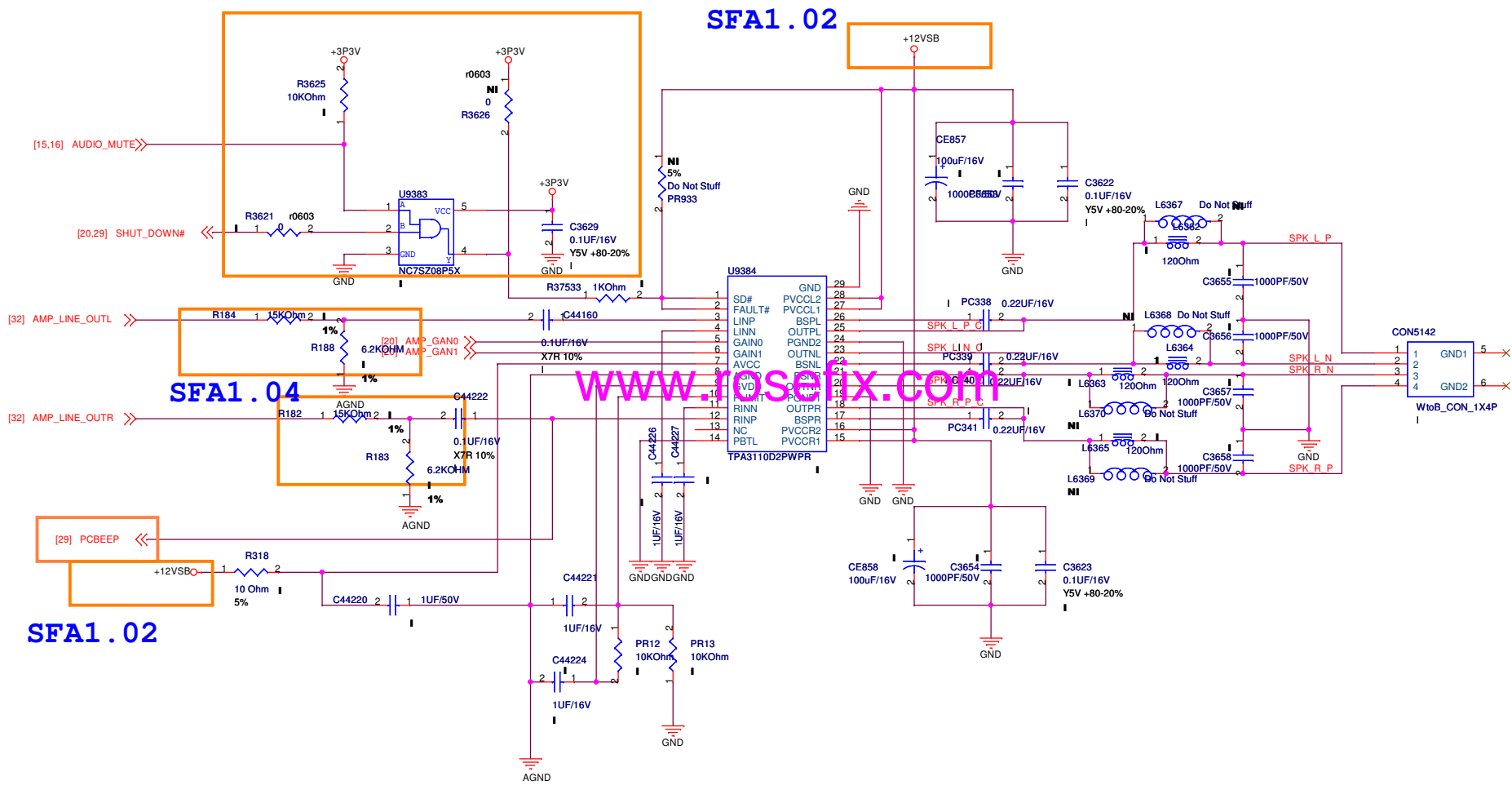


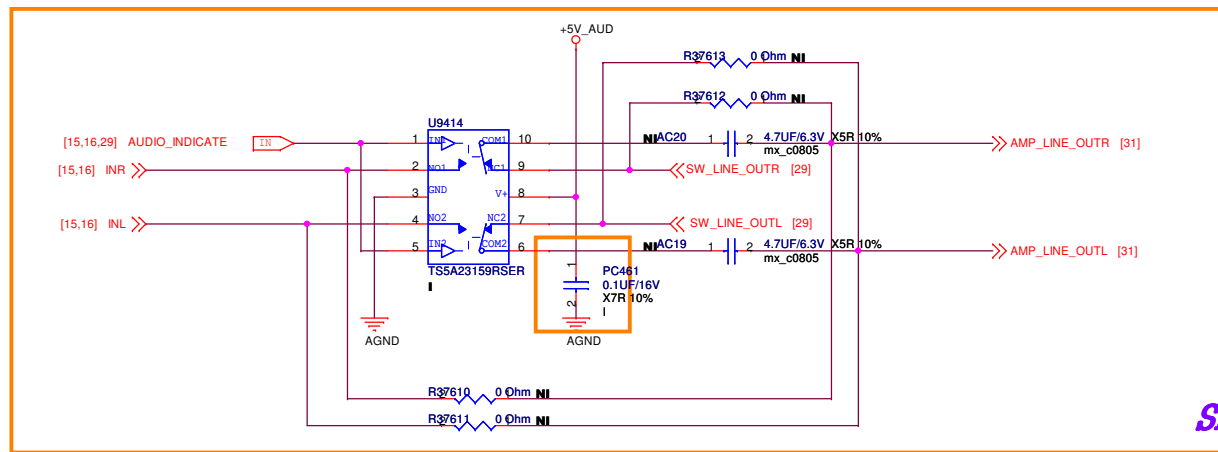


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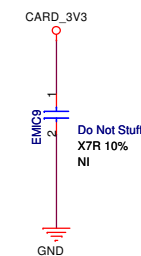
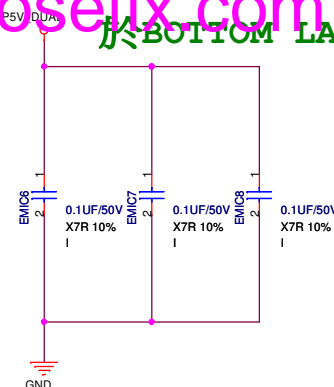
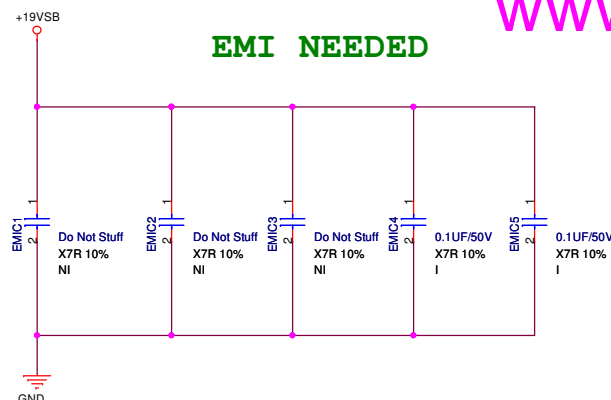
SPA1.04

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於BOTTOM LAYER 上

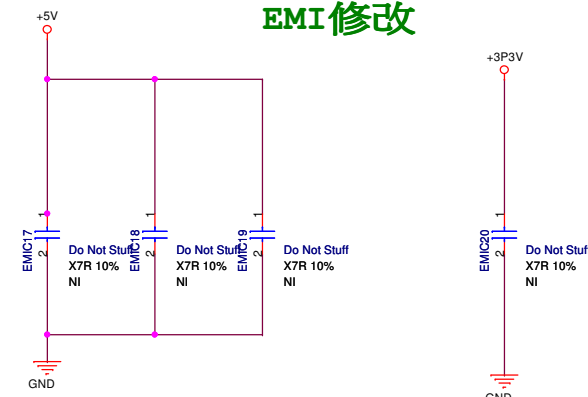
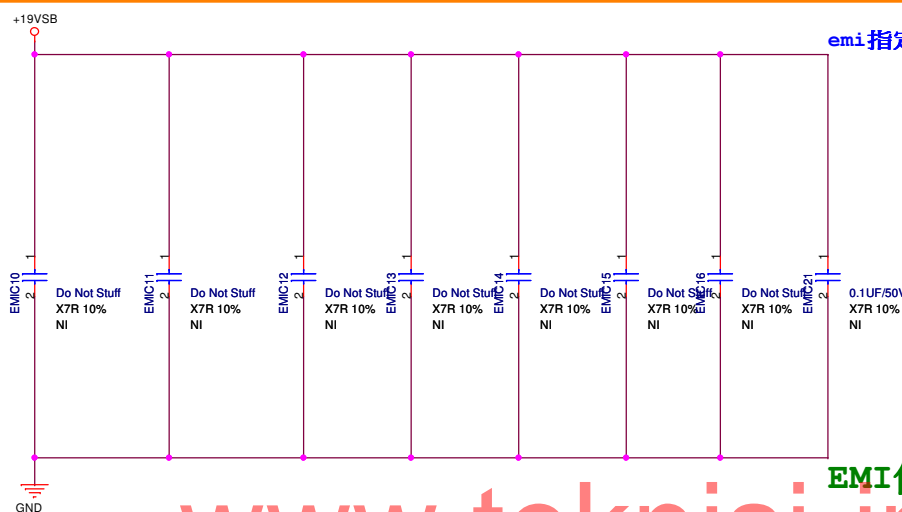
於TOP LAYER 上

EMI NEEDED



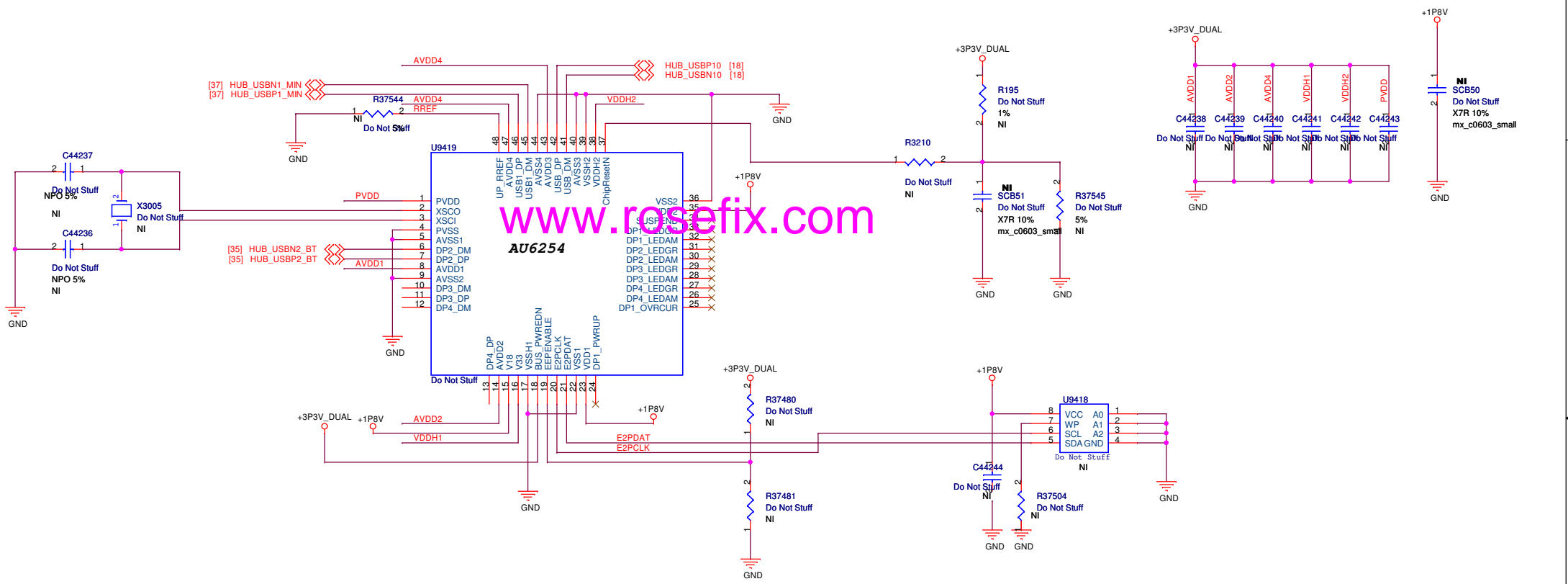
emi指定位置

EMI修改



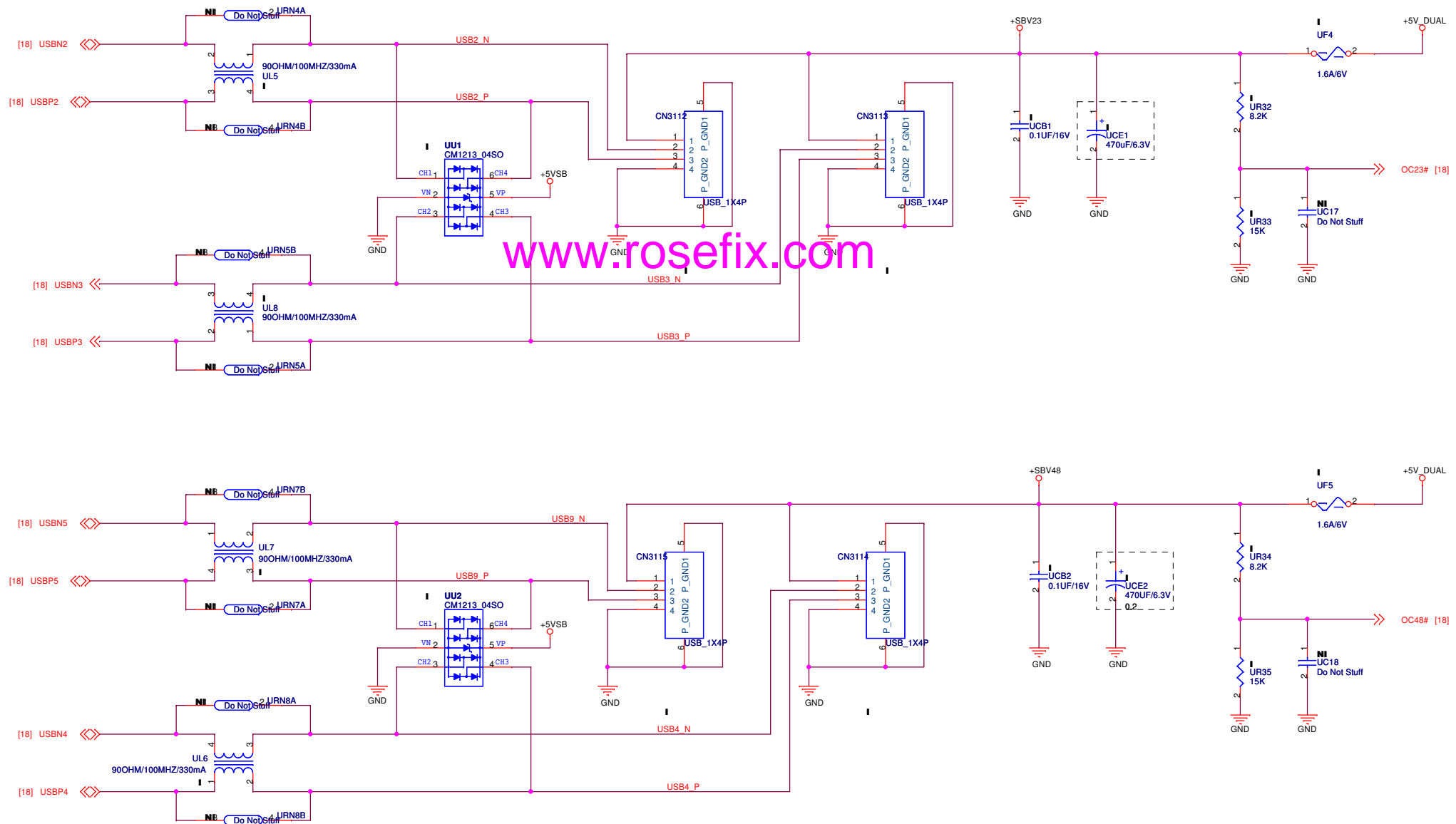
EMI修改

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整頁修改過

Rear USB2.0 *4



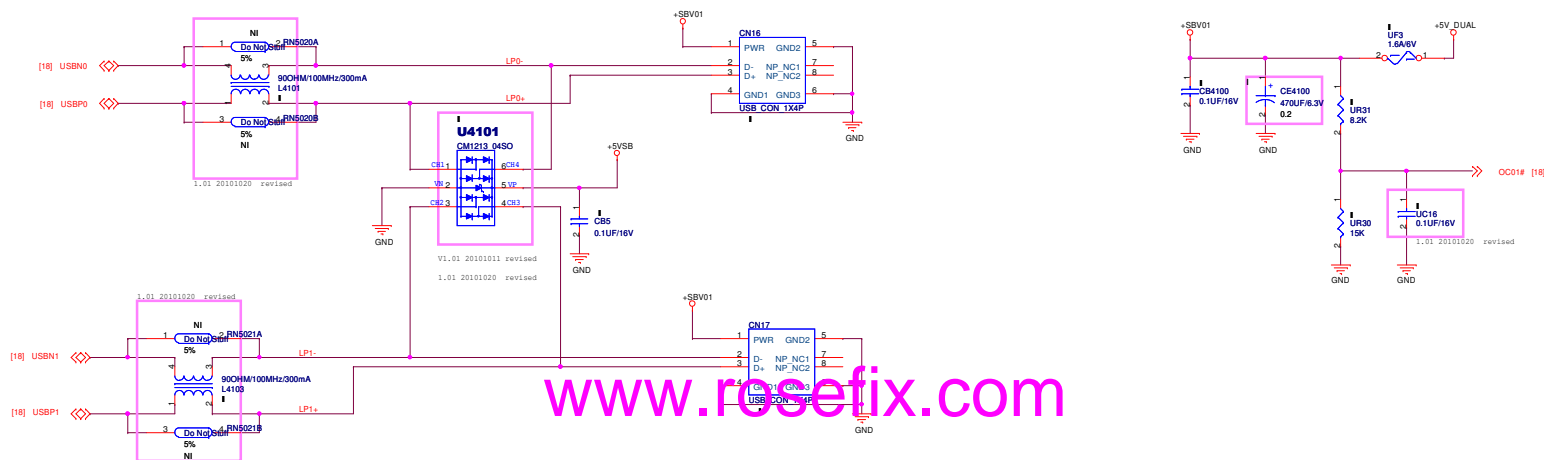
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PEGATRON		Title : Rear USB	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet 34 of 79	

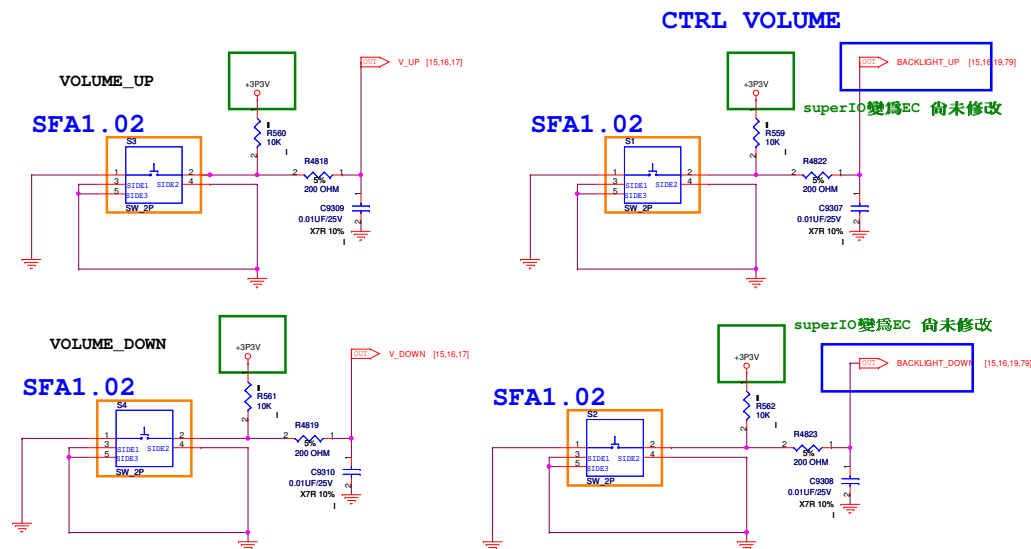
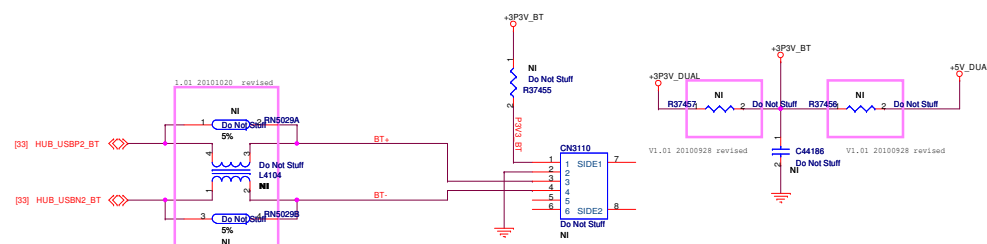
Side USB

已修改過

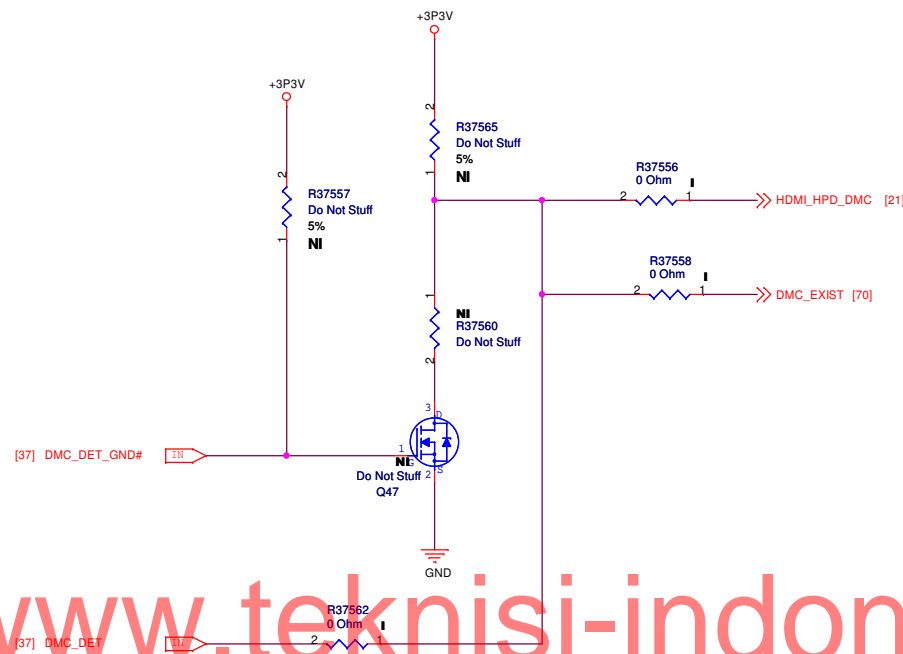
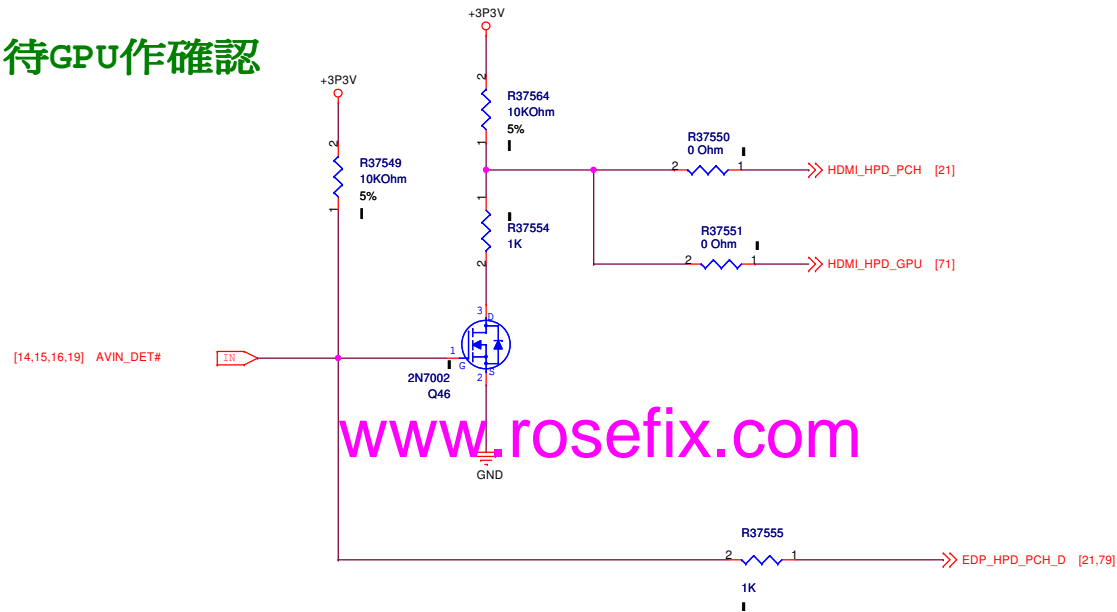


另外增加
Internal I/O
BLUE TOOTH

the DMC device connected BT symbols is needed



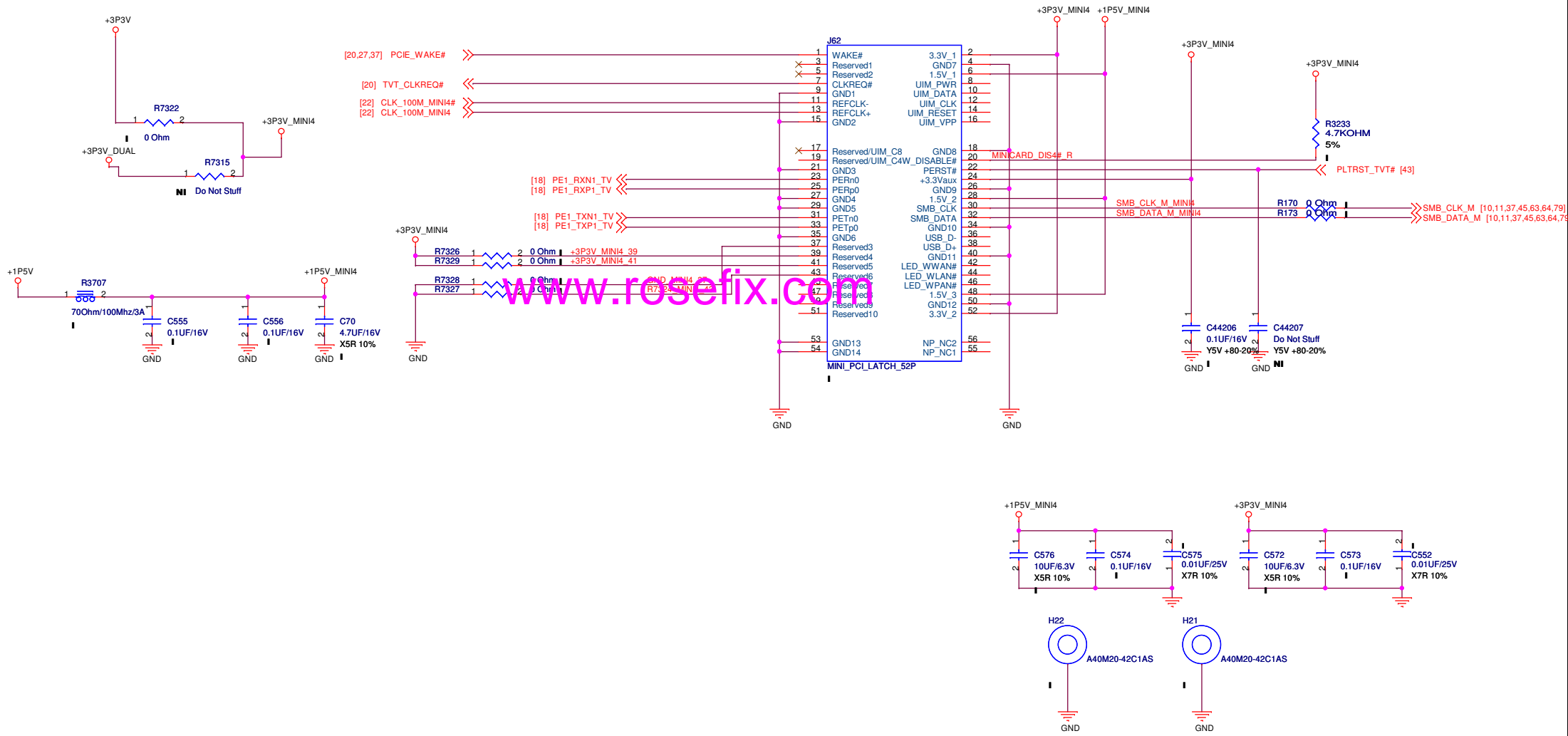
待GPU作確認



0413

PEGATRON		Title : HPD DET	
Size A3		Engineer: Jerry, Hsuan	
Date: Wednesday, April 27, 2011	Project Name	IPPSB-FA	
Rev 1.01	Sheet 36	of 79	



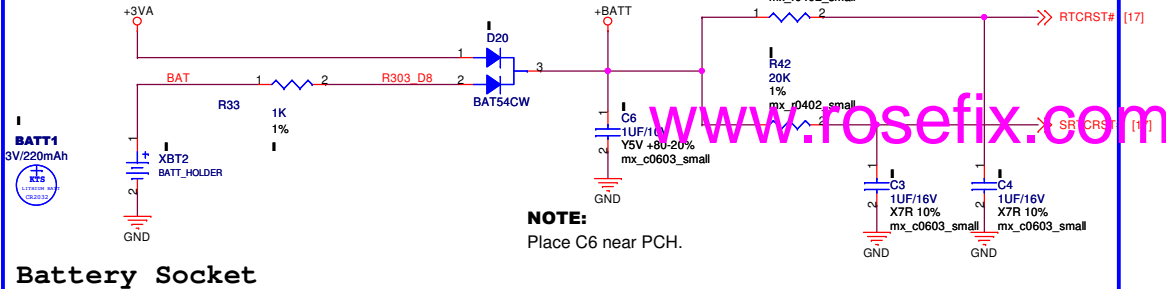


CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT

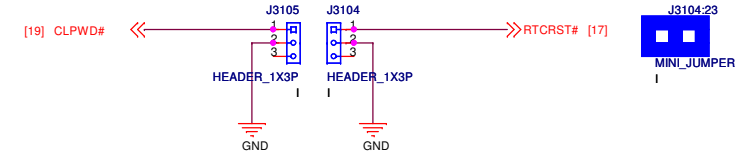
更換SCOTT的

External RTC Circuitry



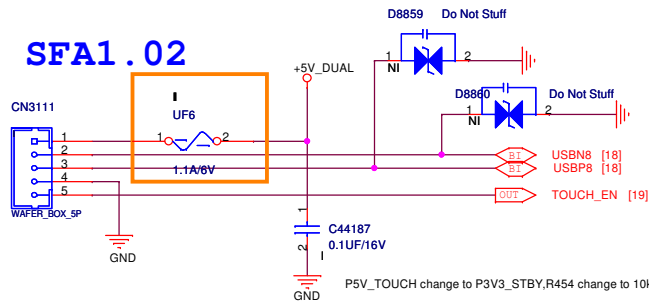
PASSWORD	
1-2	CLEAR
2-3	Default

CMOS RTC	
1-2	CLEAR
2-3	Default



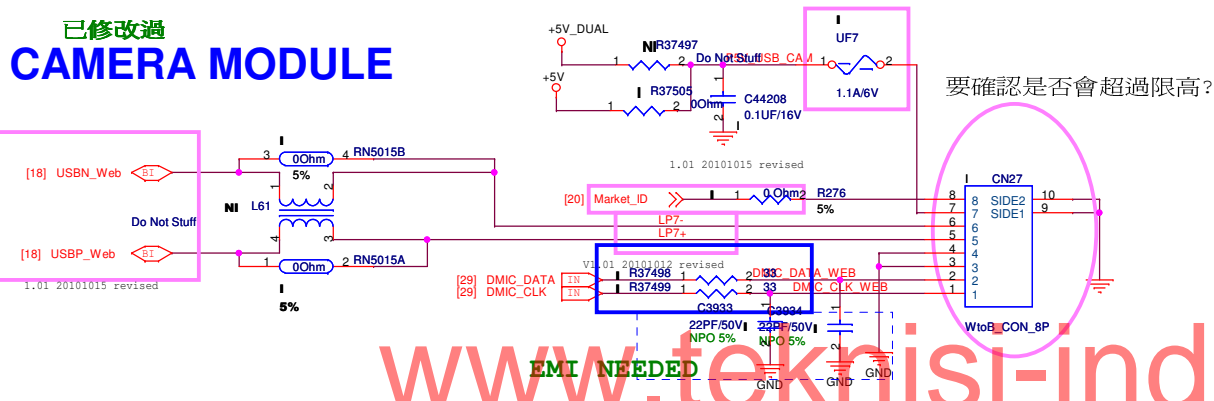
TOUCH

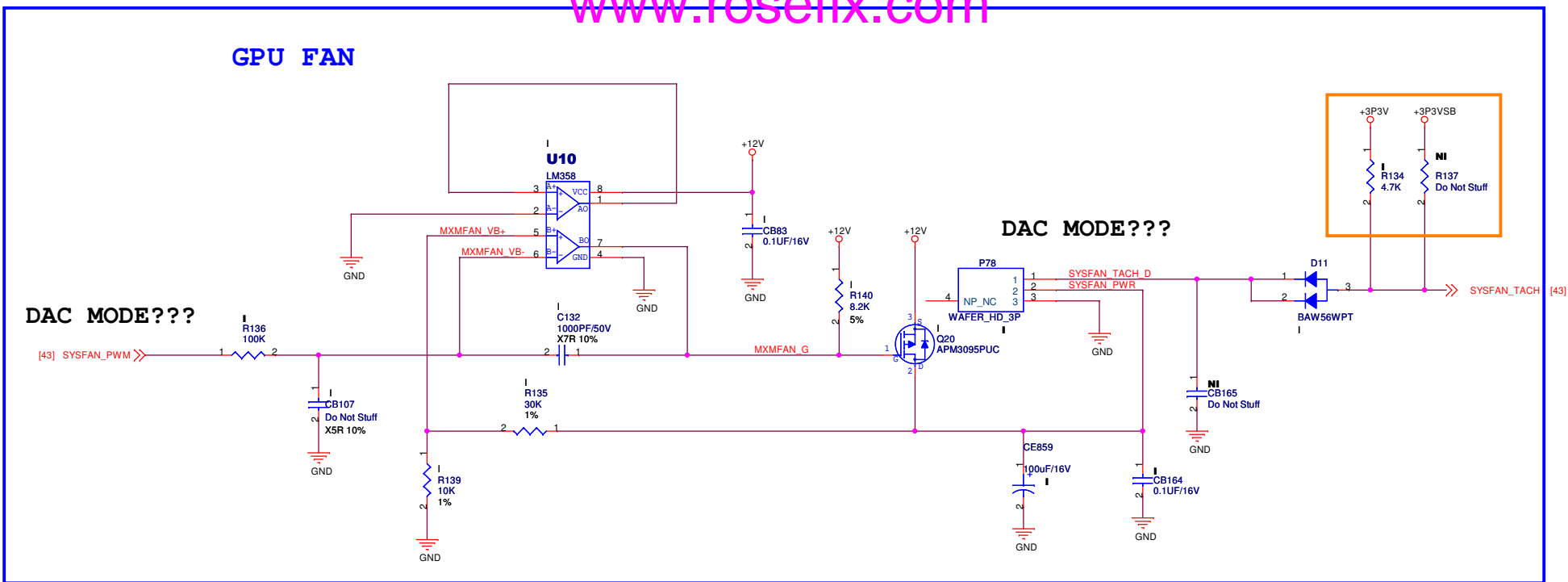
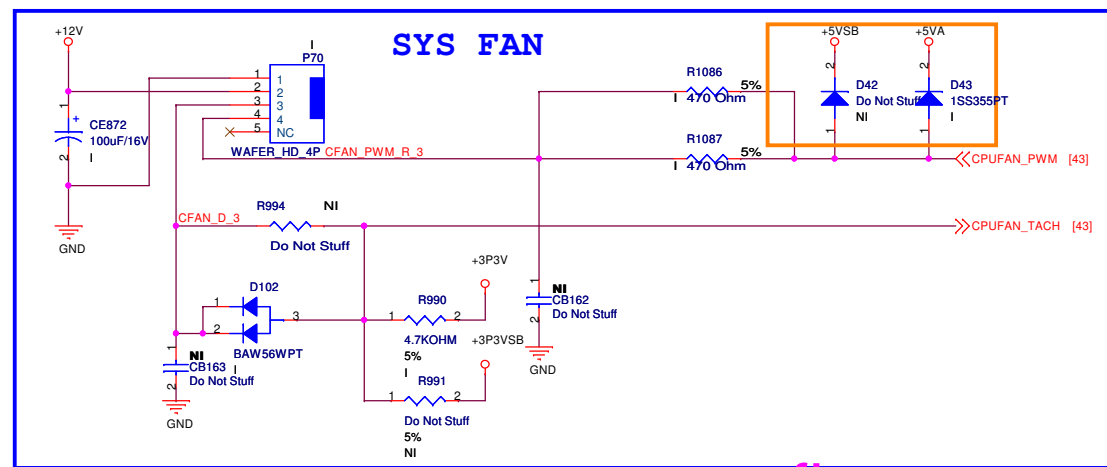
SFA1.02



SFA1.03

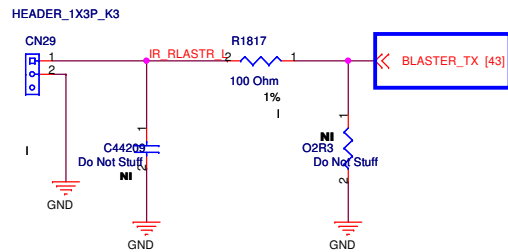
已修改過 CAMERA MODULE





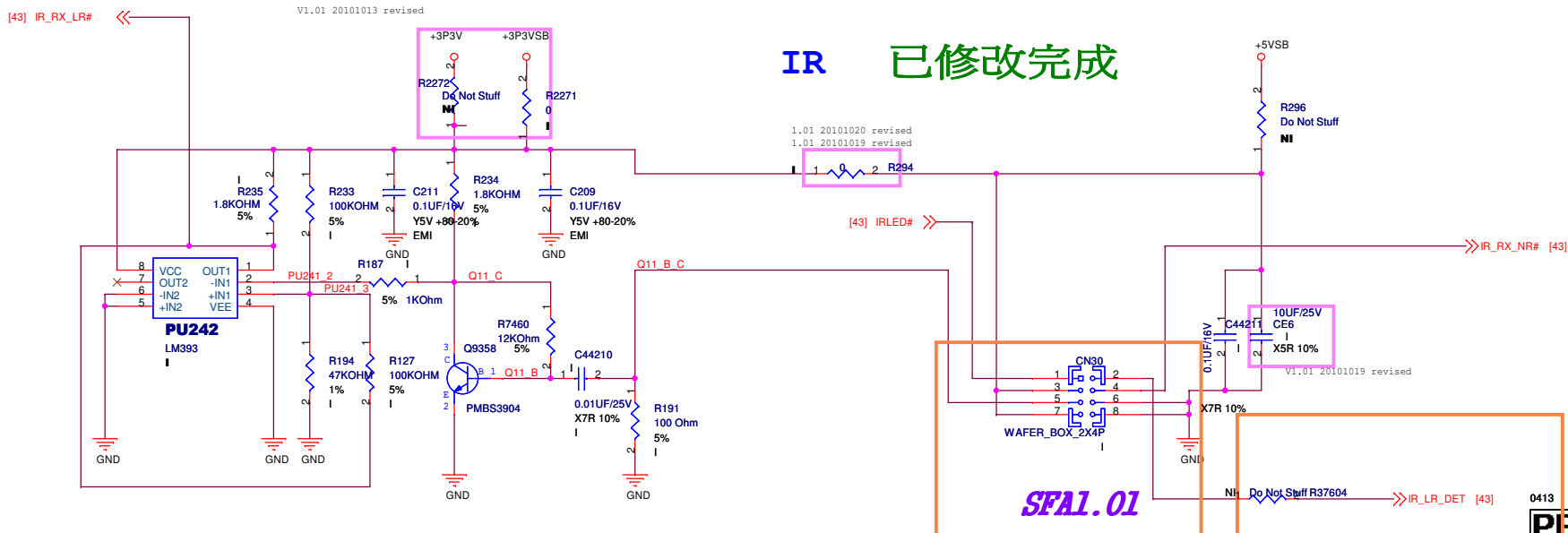
線條未改

IR Blaster



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IR 已修改完成

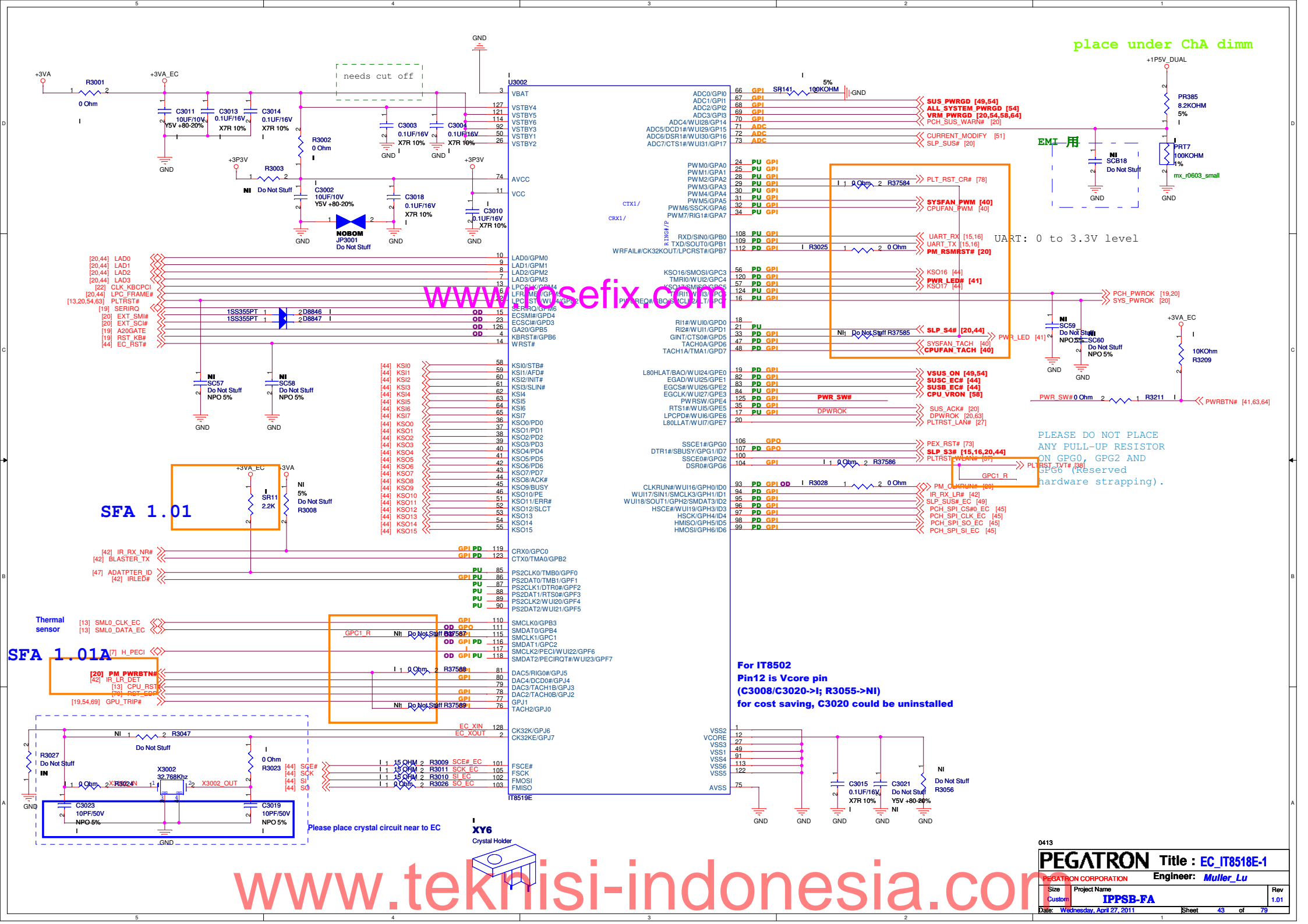


SFA1.01

SFA1.01A

0413		PEGATRON Title : IR LEDs	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet 42 of 79	

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place under ChA dimm

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EMI 用

UART: 0 to 3.3V level

PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG3 (Reserved hardware strapping).

For IT8502
Pin12 is Vcore pin
(C3008/C3020->I; R3055->NI)
for cost saving, C3020 could be uninstalled

[illegible]

For Instant Key & Switch

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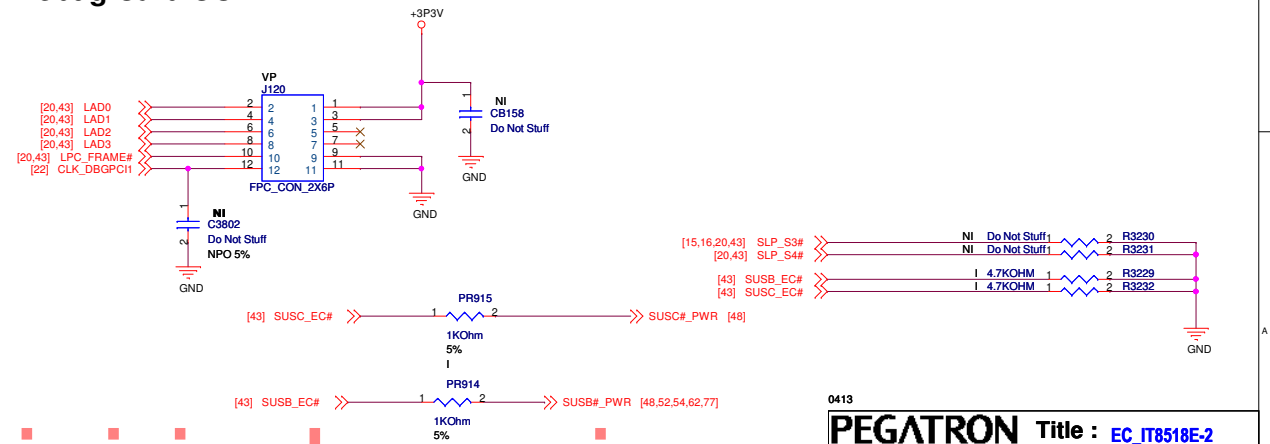
12/13 CN3101~7
I-->VP

Do Not Surf 2
Do Not Surf 4
Do Not Surf 6
Do Not Surf 8
Do Not Surf 10
Do Not Surf 12
Do Not Surf 14
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Do Not Surf 86
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Do Not Surf 94
Do Not Surf 96
Do Not Surf 98
Do Not Surf 100

1 CN3101A
3 CN3101B
5 CN3101C
7 CN3101D
9 CN3101E
11 CN3101F
13 CN3101G
15 CN3101H
17 CN3101I
19 CN3101J
21 CN3101K
23 CN3101L
25 CN3101M
27 CN3101N
29 CN3101O
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33 CN3101Q
35 CN3101R
37 CN3101S
39 CN3101T
41 CN3101U
43 CN3101V
45 CN3101W
47 CN3101X
49 CN3101Y
51 CN3101Z
53 CN3102A
55 CN3102B
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61 CN3102E
63 CN3102F
65 CN3102G
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127 CN3103L
129 CN3103M
131 CN3103N
133 CN3103O
135 CN3103P
137 CN3103Q
139 CN3103R
141 CN3103S
143 CN3103T
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285 CN3106M
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289 CN3106O
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317 CN3107C
319 CN3107D

J3103
VP

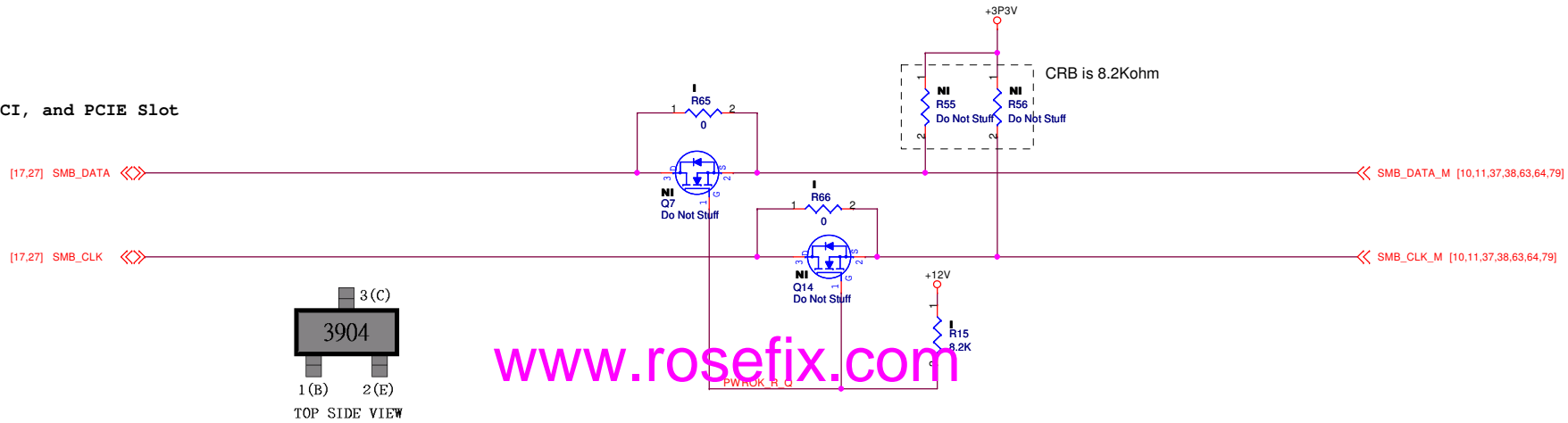
GND



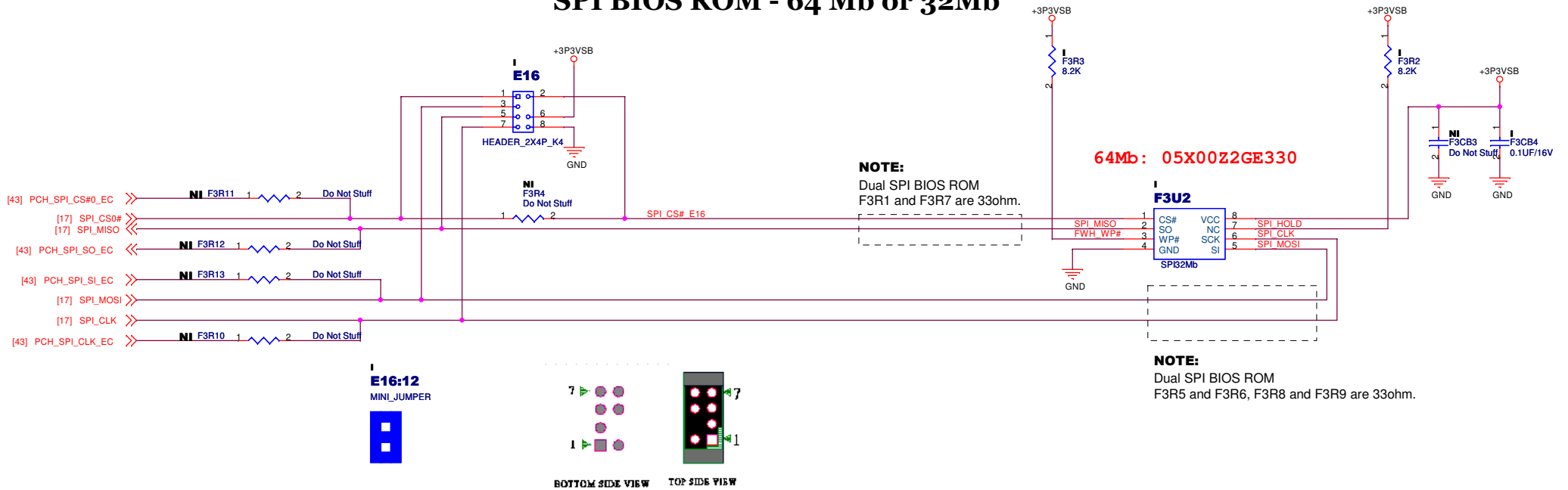
PEGATRON		Title : EC_IT8518E-2	
PEGATRON CORPORATION		Engineer: Muller_Lu	
Size Custom	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011	Sheet 44	of 79	

SM BUS Control

To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb



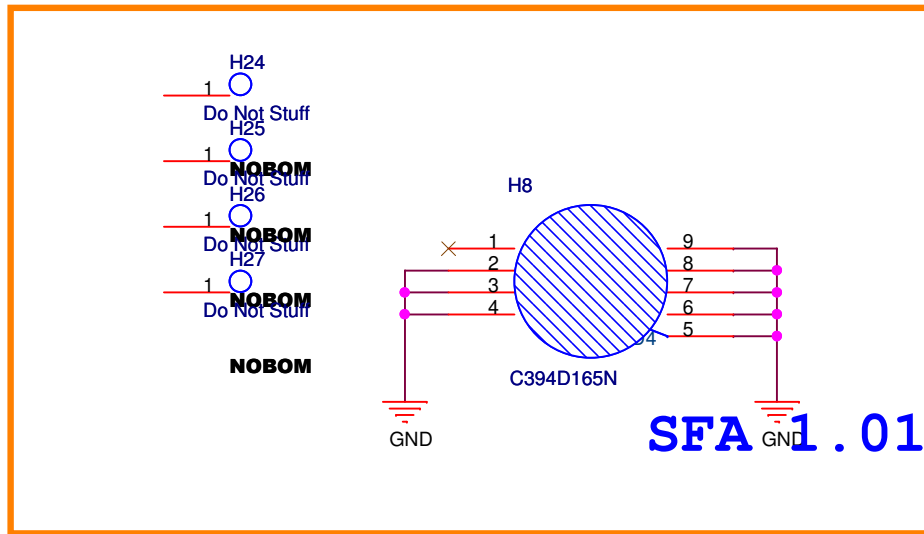
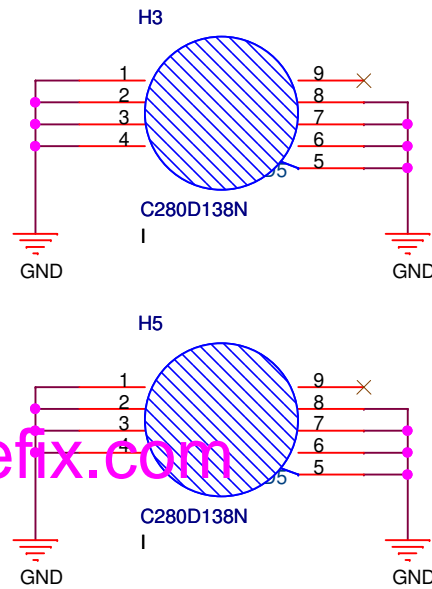
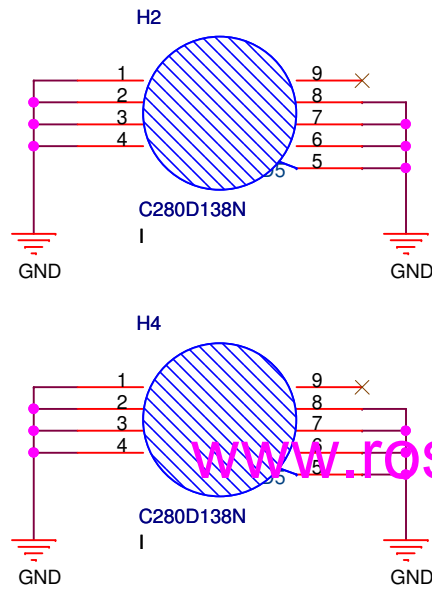
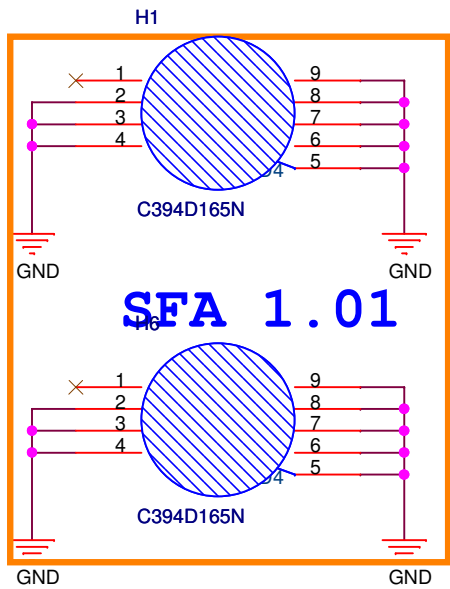
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SM BUS & SPI ROM**

PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPPSB-FA	1.01

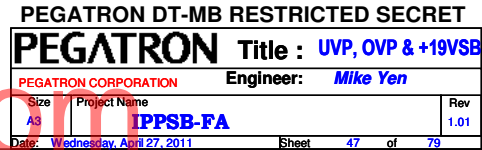
Date: Wednesday, April 27, 2011 Sheet 45 of 79



0413

PEGATRON		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name		Rev
A	IPISB-FA		1.01
Date: Wednesday, April 27, 2011		Sheet	46 of 79

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+19VSB
lin=5.95A
Trace Width>240mil

+19VSB
Iin=3.25A
Trace Width>130mil

+5VSB
I_{max}=18.07A
TDC=12.65A
Trace Width>730mil

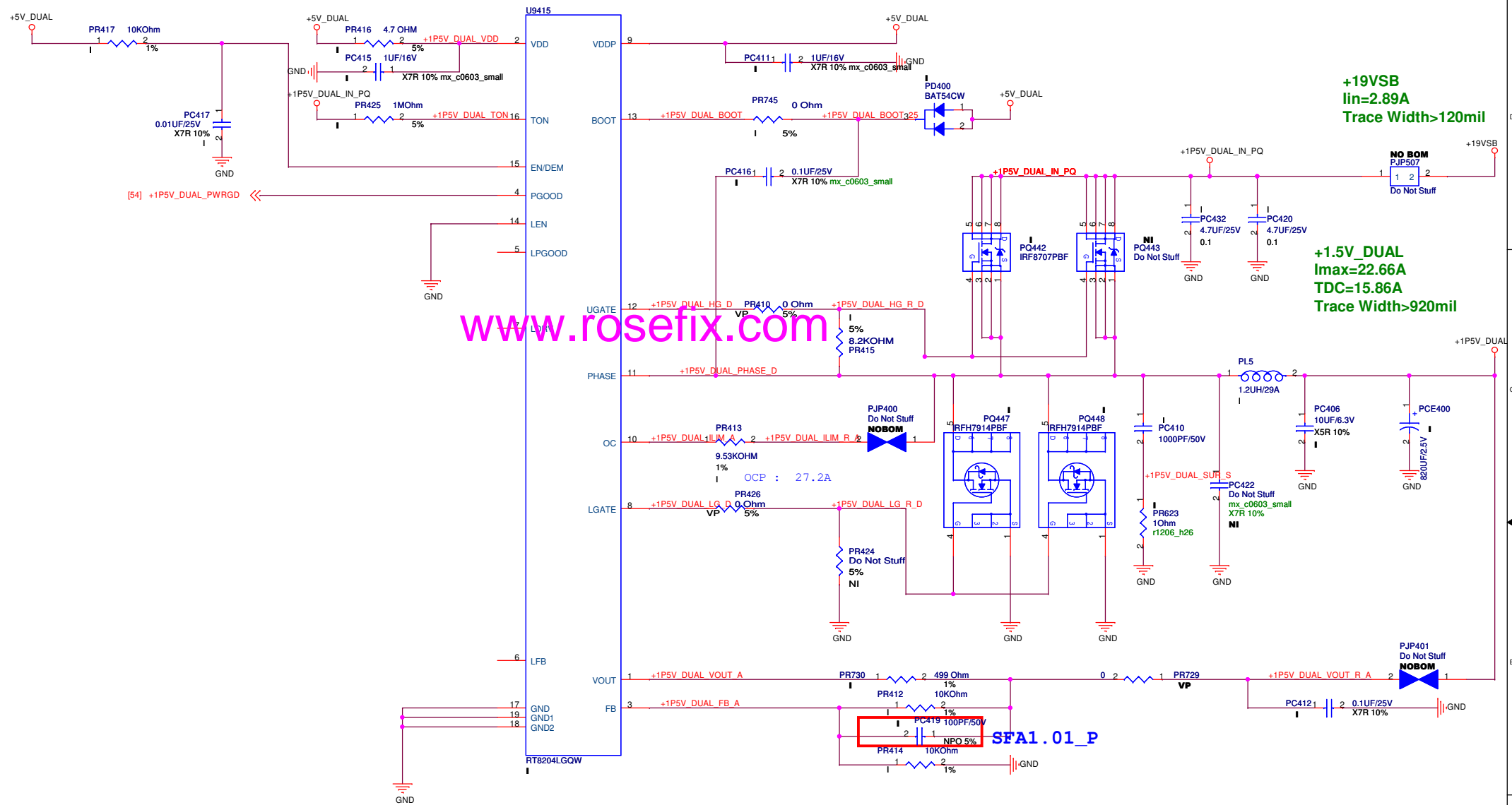
+3P3VSB
I_{max}=16.63A
TDC=11.65A
Trace Width>680mil

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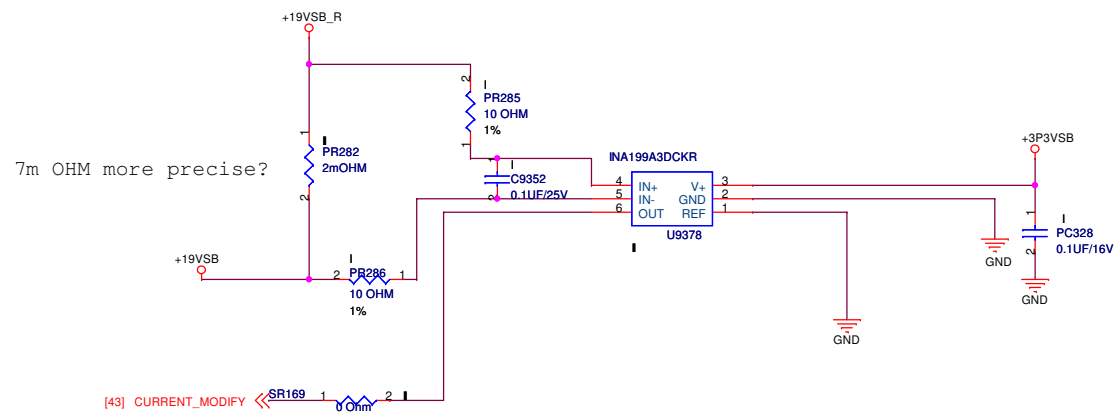
PEGATRON		Title : +3VA&+3VSB&+5VSB
PEGATRON CORPORATION		Engineer: Mike Yen
Size	Project Name	Rev
Custom	IPPSB-FA	1.01
Date: Wednesday, April 27, 2011		Sheet 49 of 79

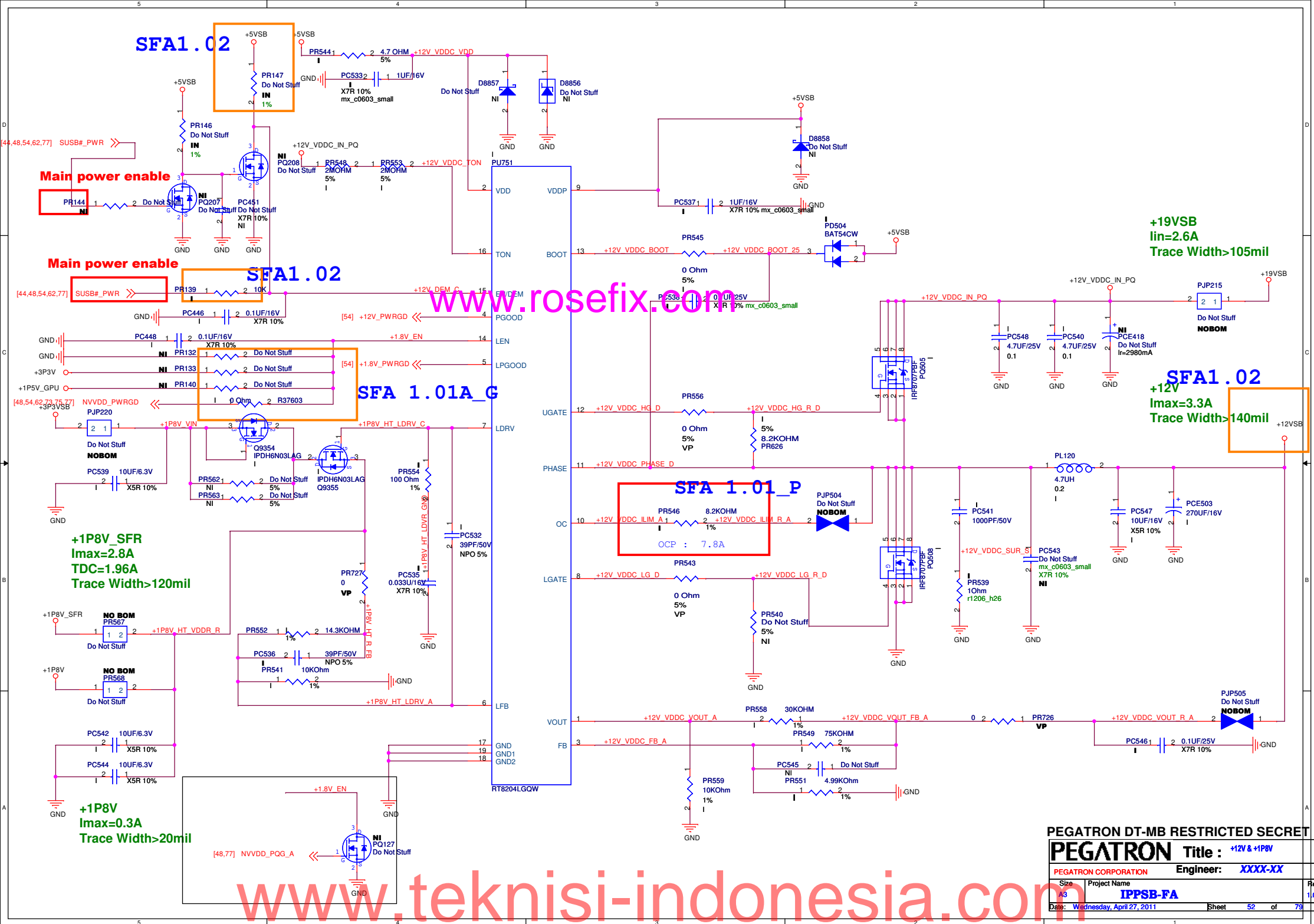
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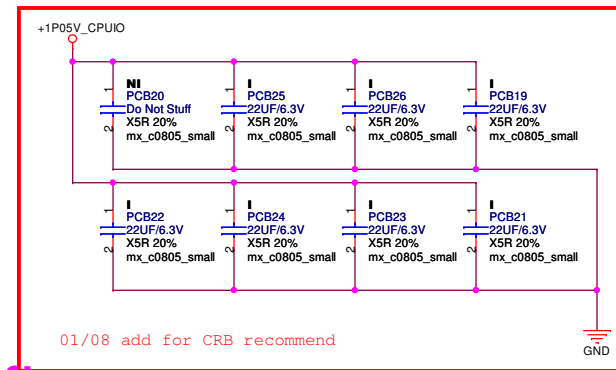
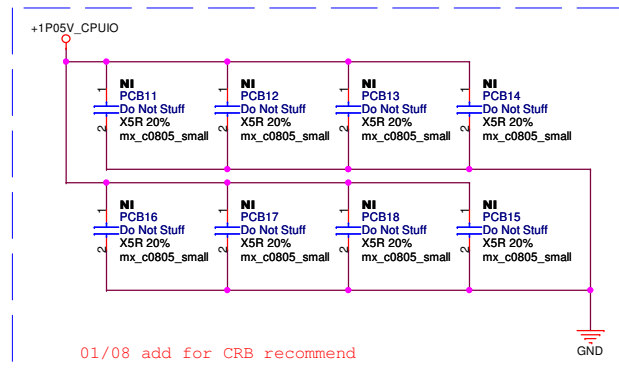
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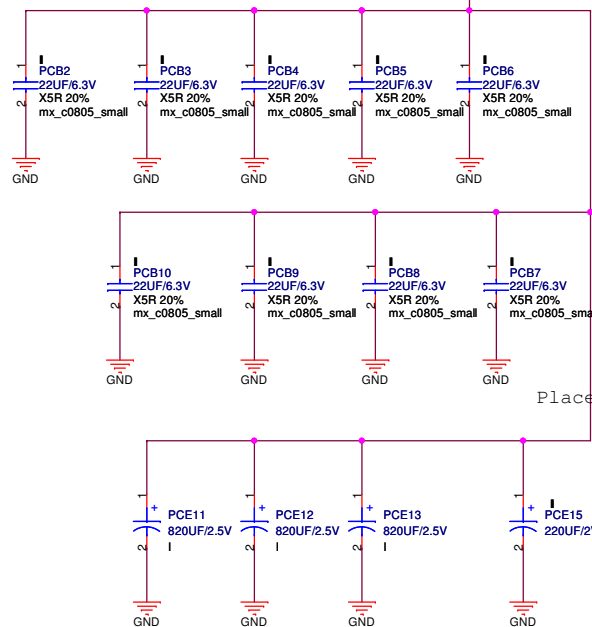








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VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	

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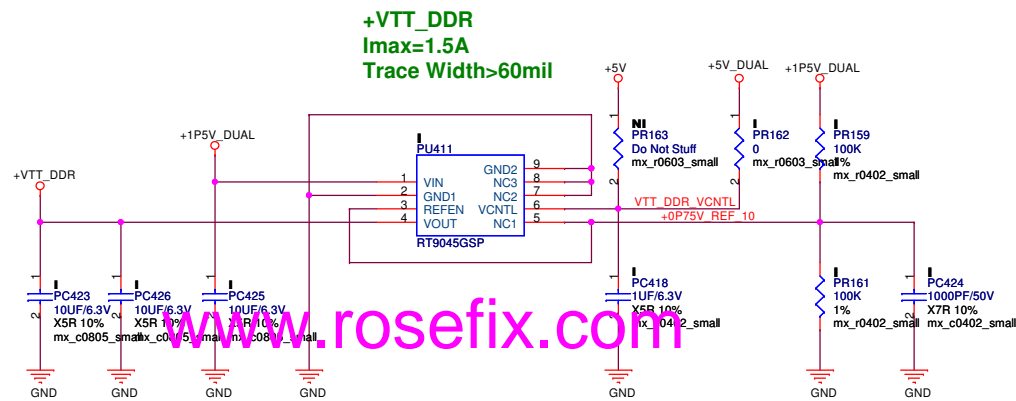
PEGATRON DT-MB RESTRICTED SECRET

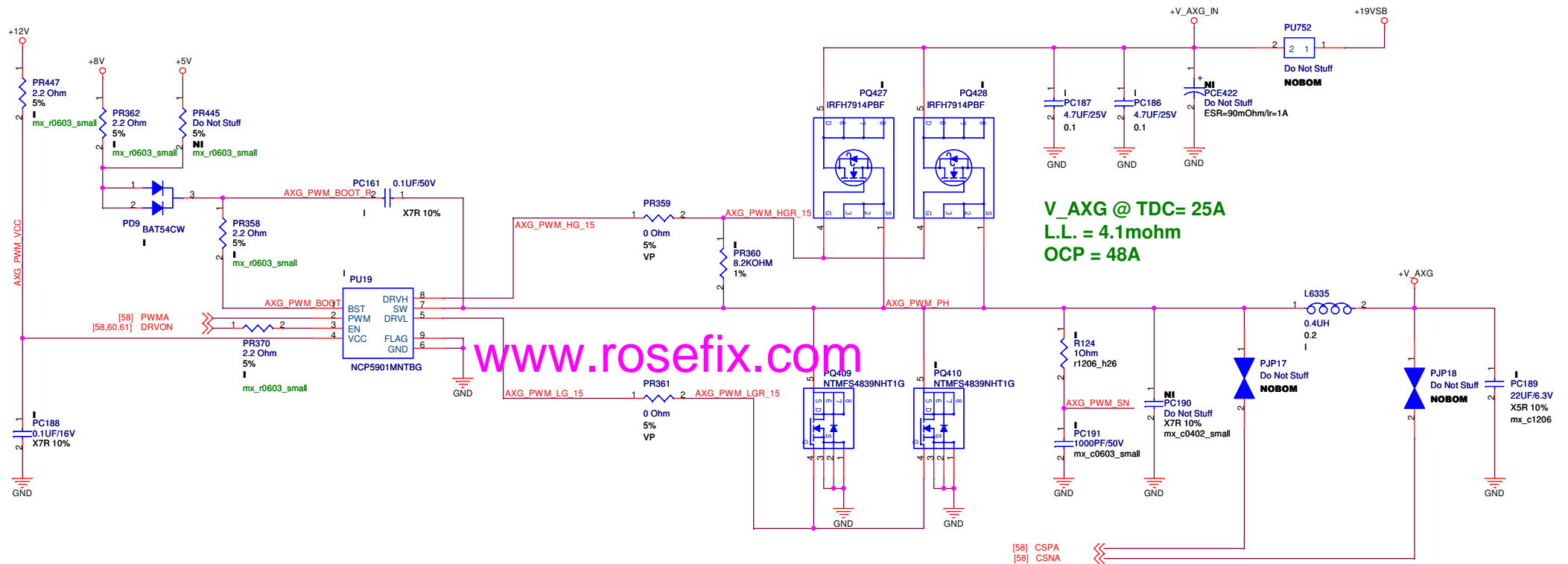
PEGATRON Title : 1P05V_CPU10 CAP

PEGATRON CORPORATION Engineer: XXXX-XX

Size: A3 Project Name: IPPSB-FA Rev: 1.01

Date: Tuesday, April 26, 2011 Sheet 55 of 79



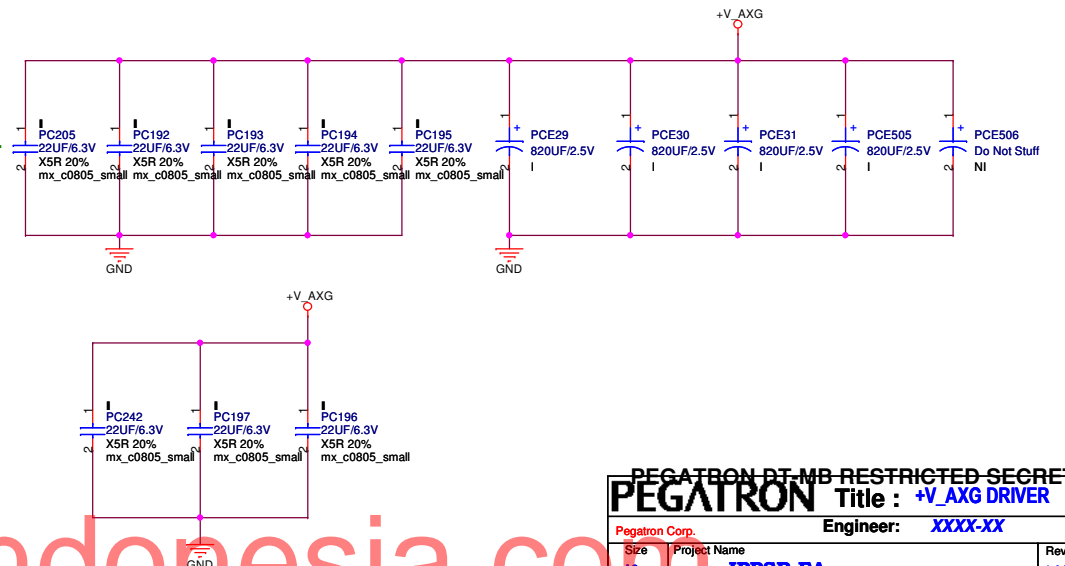


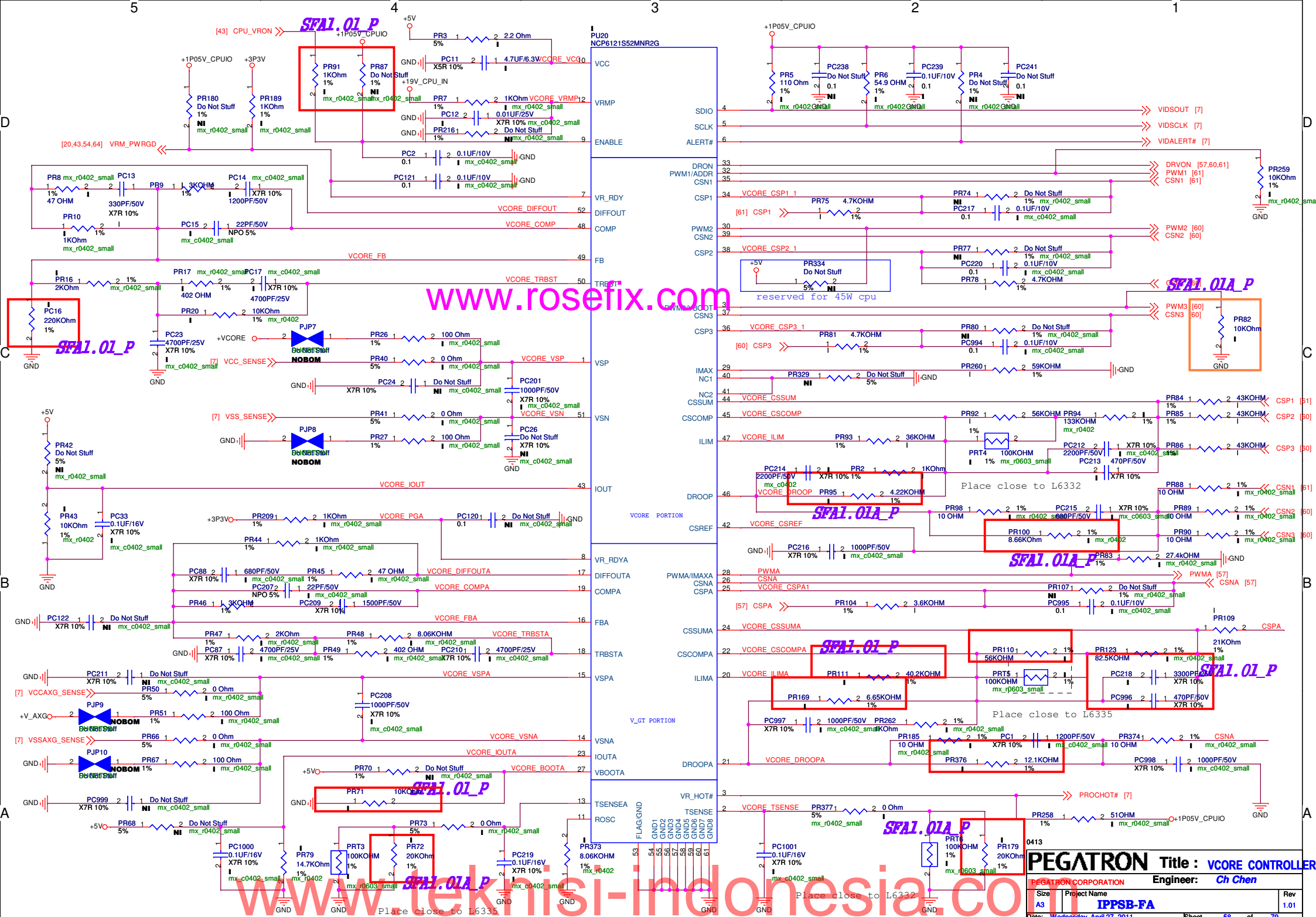
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



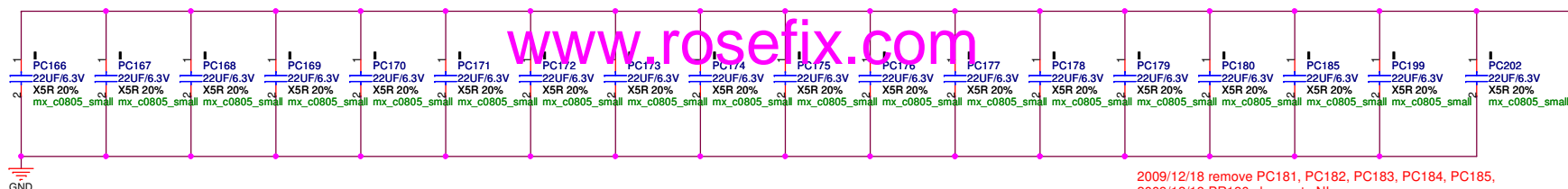
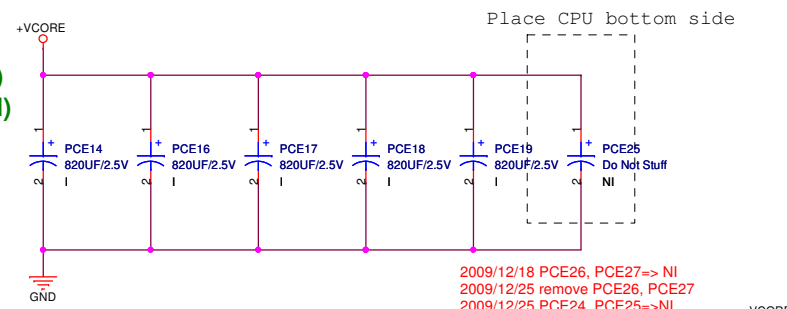


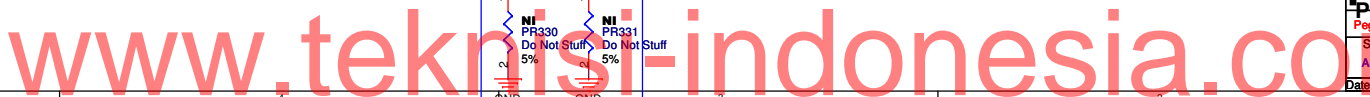
Output CAP

Table 30-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)





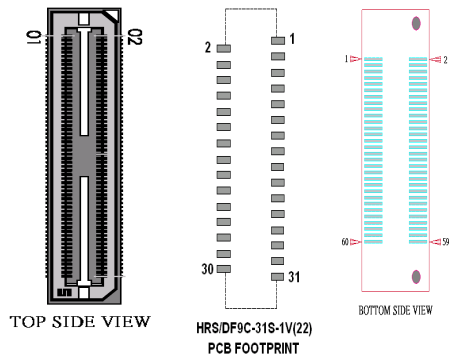
BOTTOM SIDE VIEW

**PEGATRON** Title : PCH XDP DEBUG

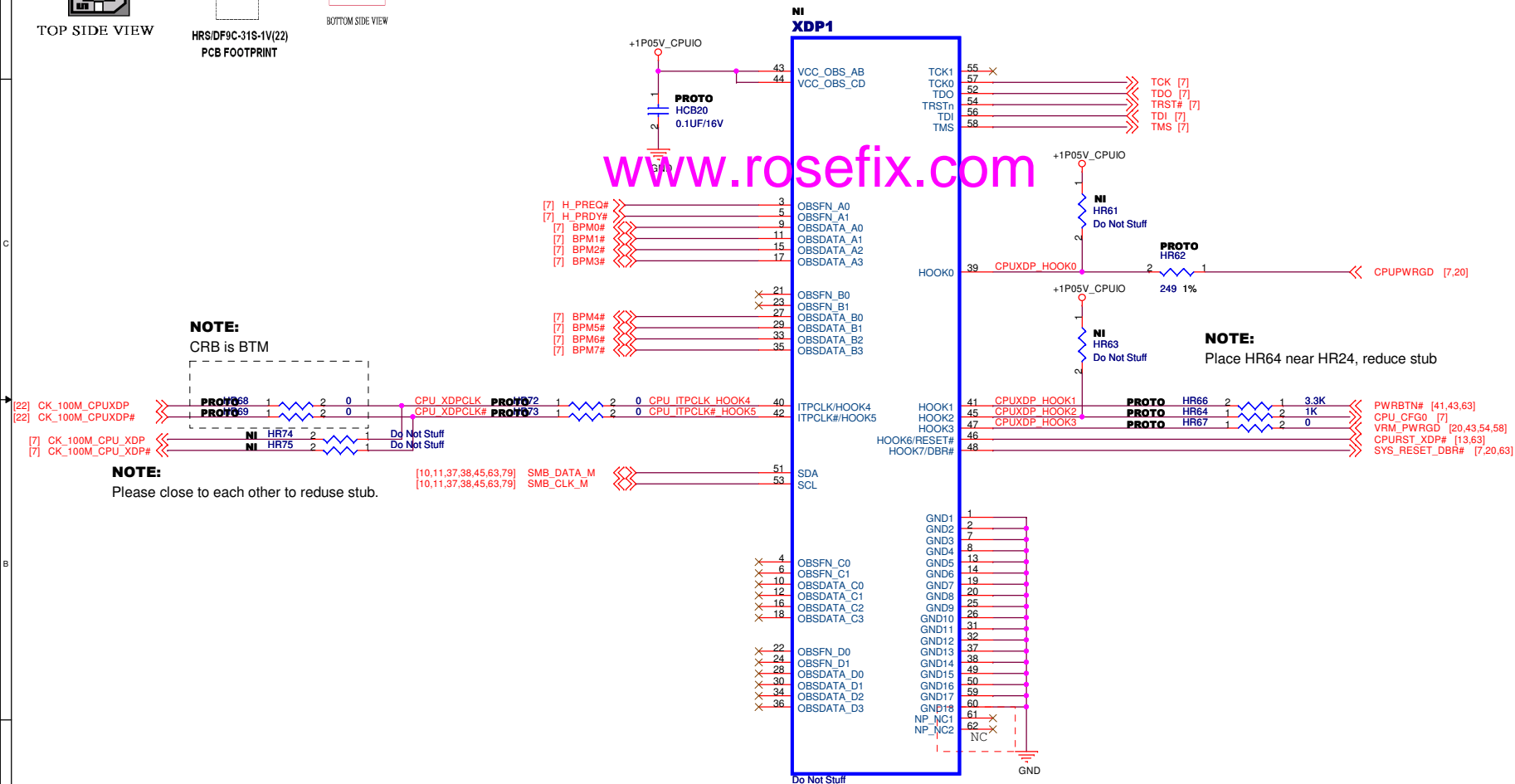
PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPPSB-FA	1.01

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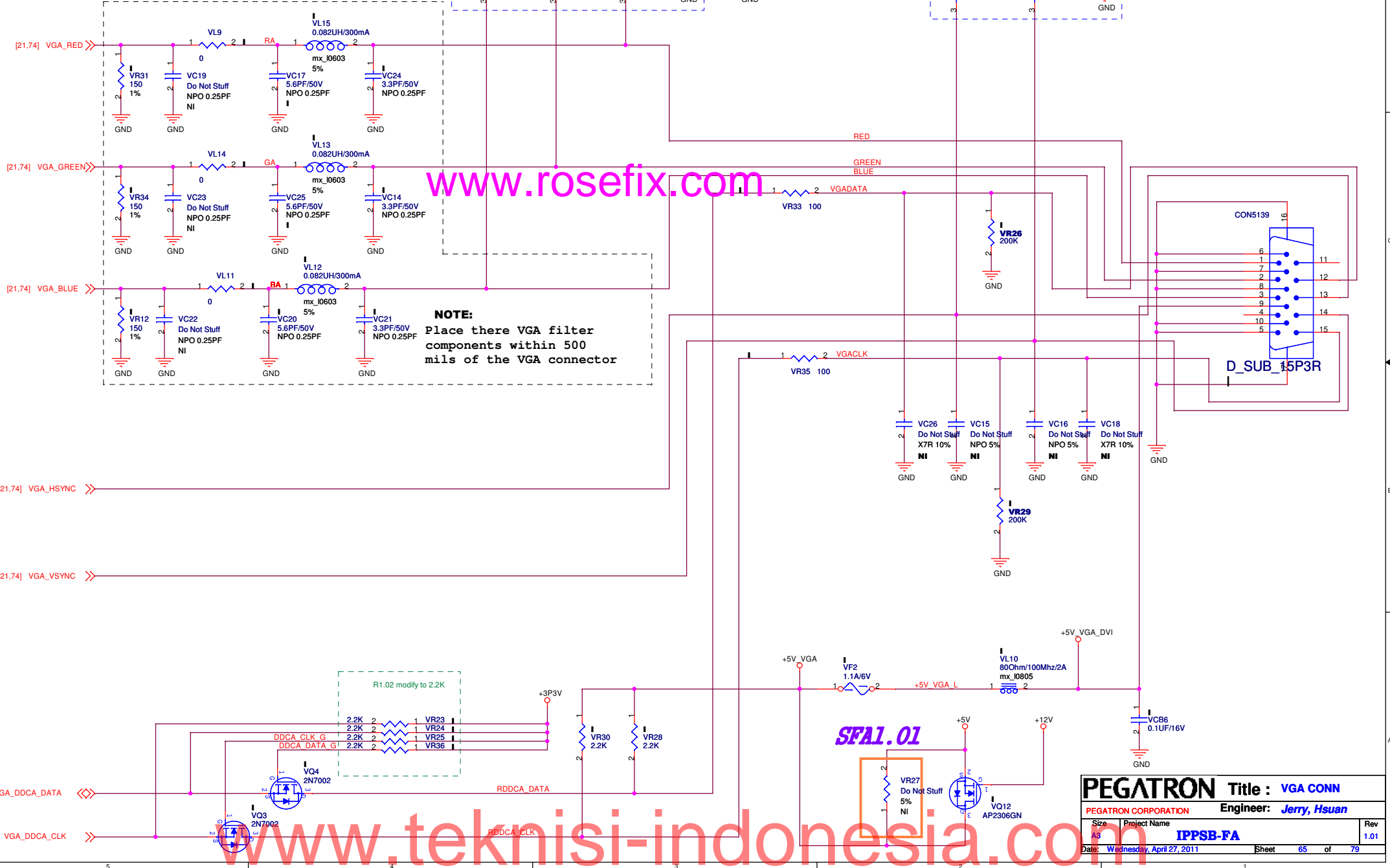
INTEL CPU XDP DEBUG PORT

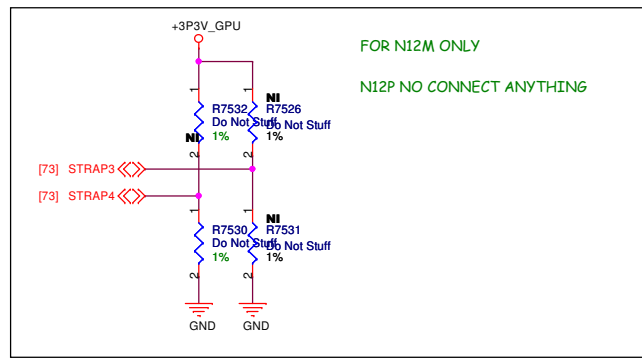
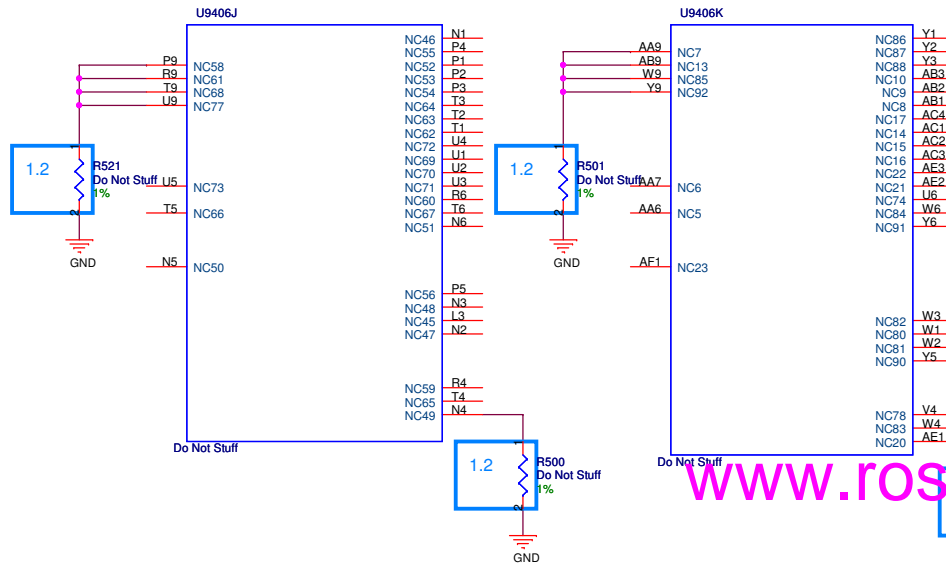


整份新增修改

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:





ROM_SI	bit0	RAM_CFG_0	16b (64Mx16 8pcs)
	bit1	RAM_CFG_1	RAM_CFG[3:0] Definitions
	bit2	RAM_CFG_2	0x2: Hynix => H5TQ1G63BFR-12C
	bit3	RAM_CFG_3	0x3: Samsung => K4W1G1646E-HC12
0x0010 : 15K PD			

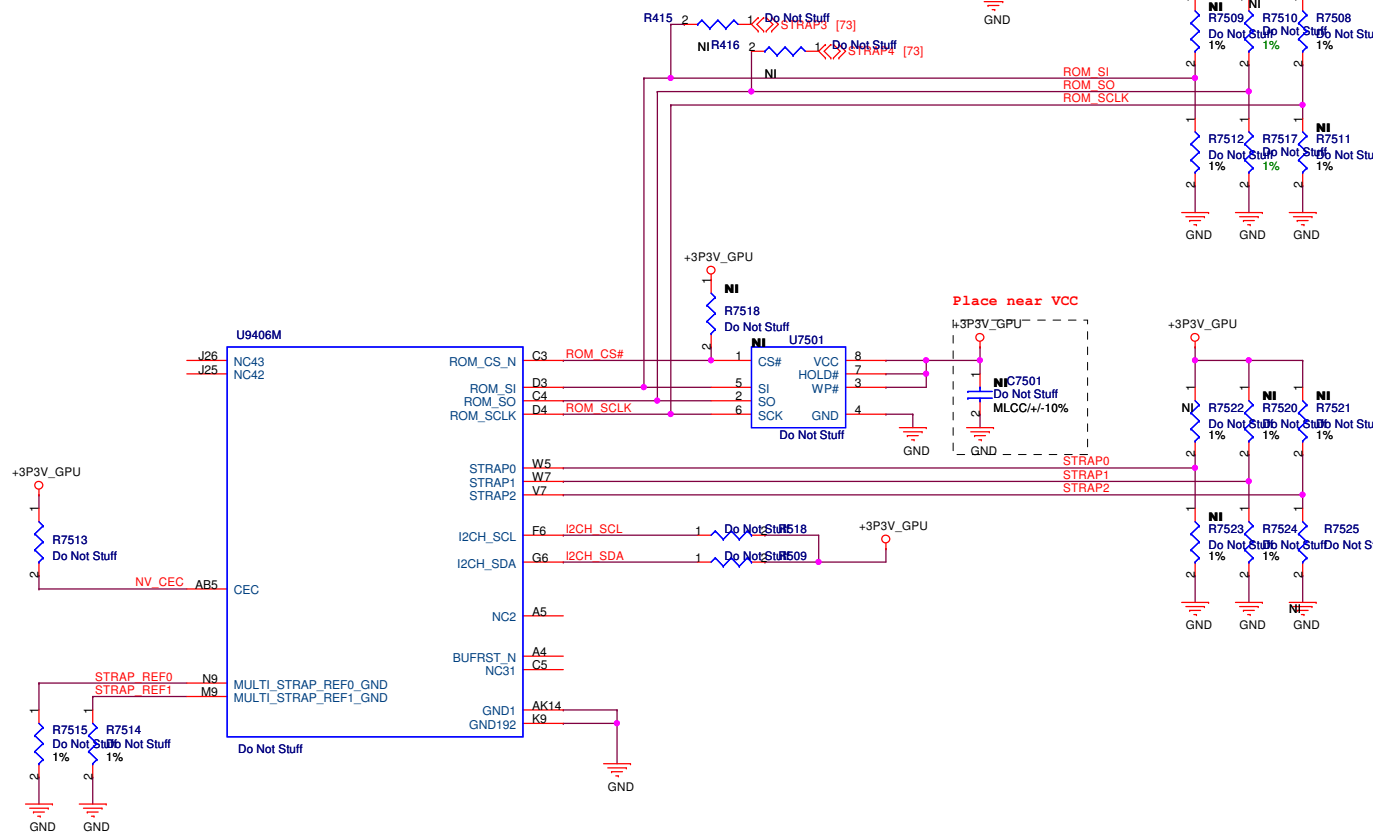
ROM_SO	bit0	VGA_DEVICE	1: VGA Device (default class code 300h)
	bit1	SMB_ALT_ADDR	0: 0x9E (default)
	bit2	FB_0_BAR_SIZE	0: 256MB (default)
	bit3	XCLK_417	0: 277M Hz (default)
different			

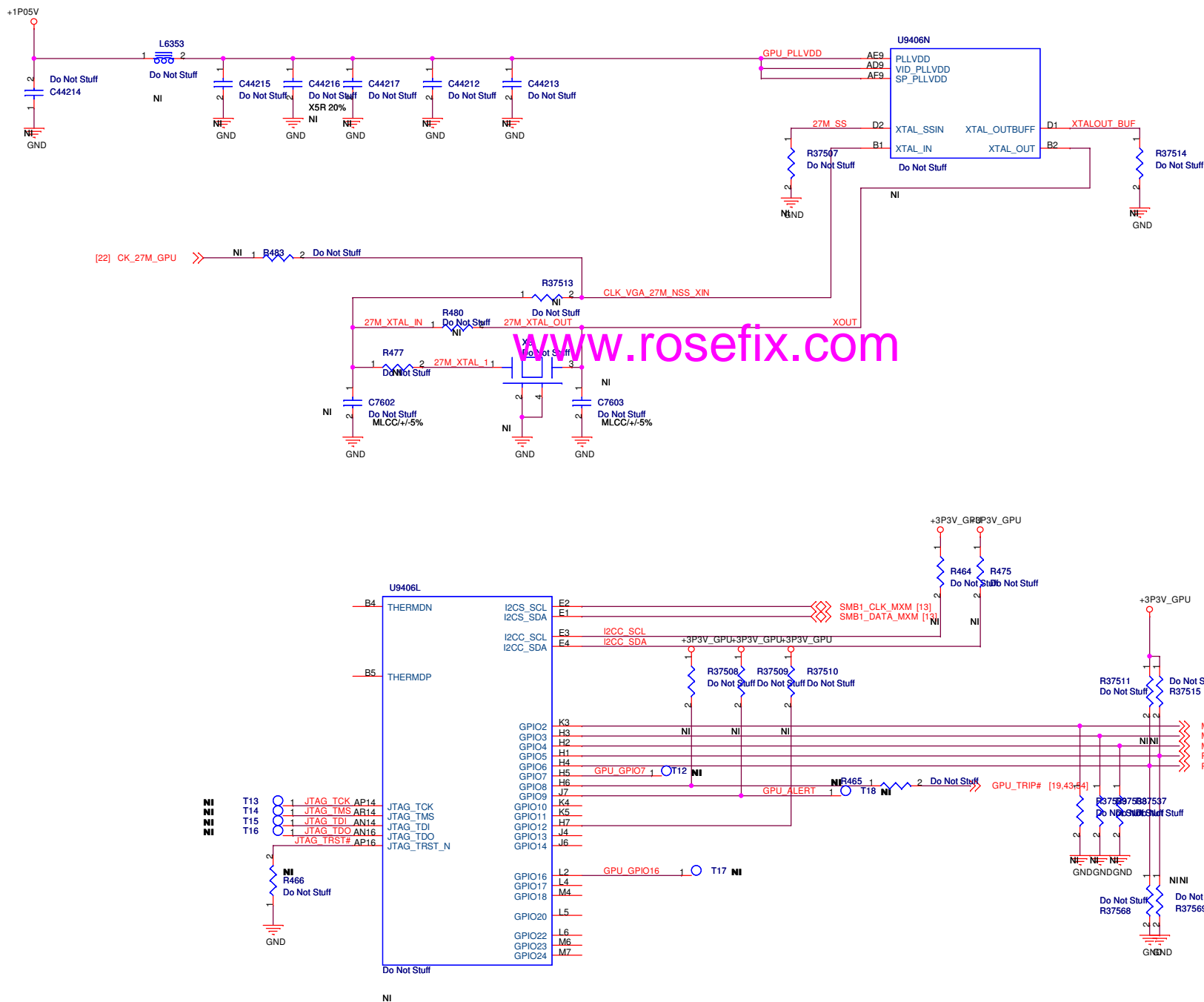
ROM_SCLK	bit0	PEX_PLL_EN_TERM	0: Disable (default)
	bit1	SLOT_CLK_CONFIG	0: GPU & MCH not share common reference clock
	bit2	SUB_VENDER	0: no vidio BIOS ROM
	bit3	PCI_DEVID_4	1: PCI_DeVID[4] => 0x0DFE bit 4 = 1
different			

STRAP0	bit0	USER_BIT0	0x0000 : 5K PD (Panels select Default 0x0000)
	bit1	USER_BIT1	
	bit2	USER_BIT2	
	bit3	USER_BIT3	

STRAP1	bit0	3GIO_PADC_F6_LUT_ADR0	0x6 : 35k PD (PCIE swing default)
	bit1	3GIO_PADC_F6_LUT_ADR1	
	bit2	3GIO_PADC_F6_LUT_ADR2	
	bit3	3GIO_PADC_F6_LUT_ADR3	

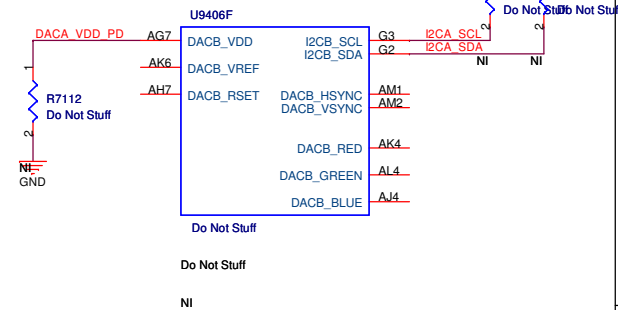
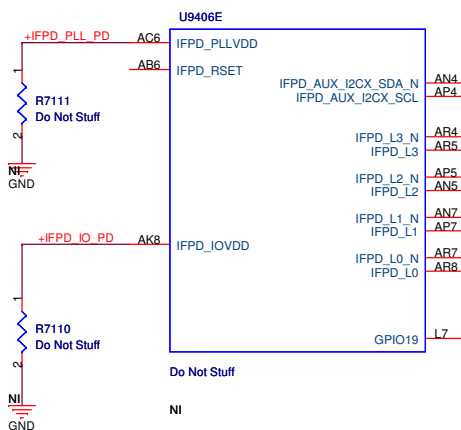
STRAP2	bit0	PCI_DEVID_0	NI2P-6E 0x0101 : 30K PD NI2M-G5 0x0100 : 30K PD
	bit1	PCI_DEVID_1	
	bit2	PCI_DEVID_2	
	bit3	PCI_DEVID_3	





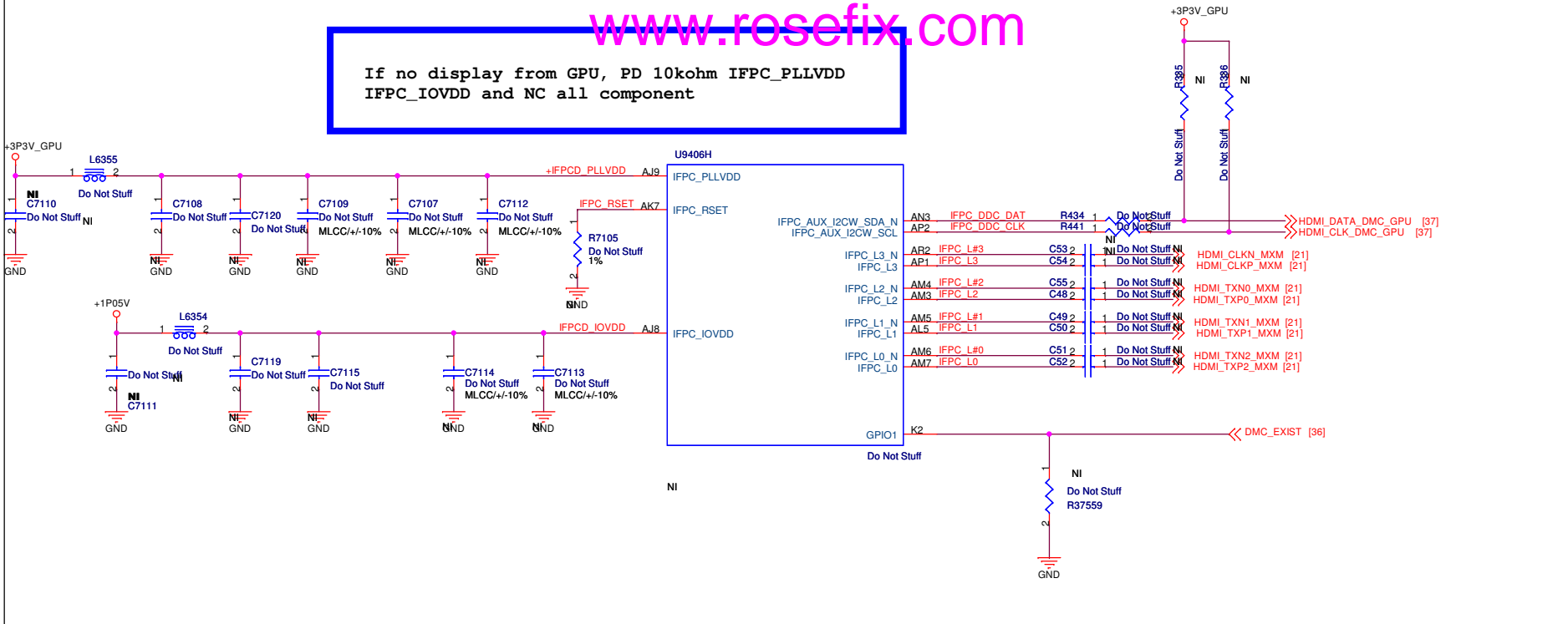
0413

PEGATRON				Title : GPU Xtal/Thermal	
PEGATRON CORPORATION				Engineer: Cryus, MJ	
Size	Project Name			Rev	
A3	IPFSB-FA			1.01	
Date: Wednesday, April 27, 2011		Sheet 69 of 79			

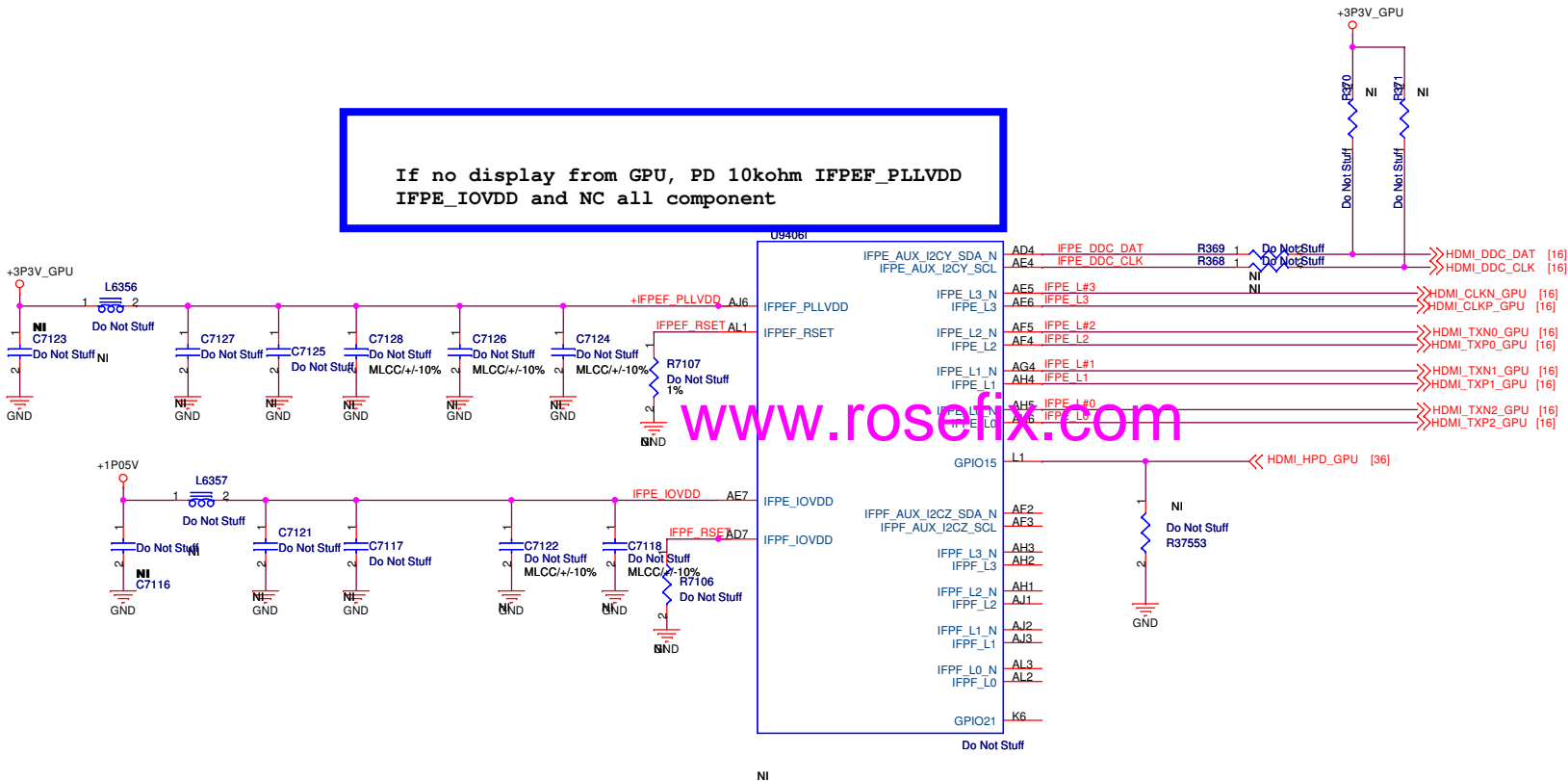


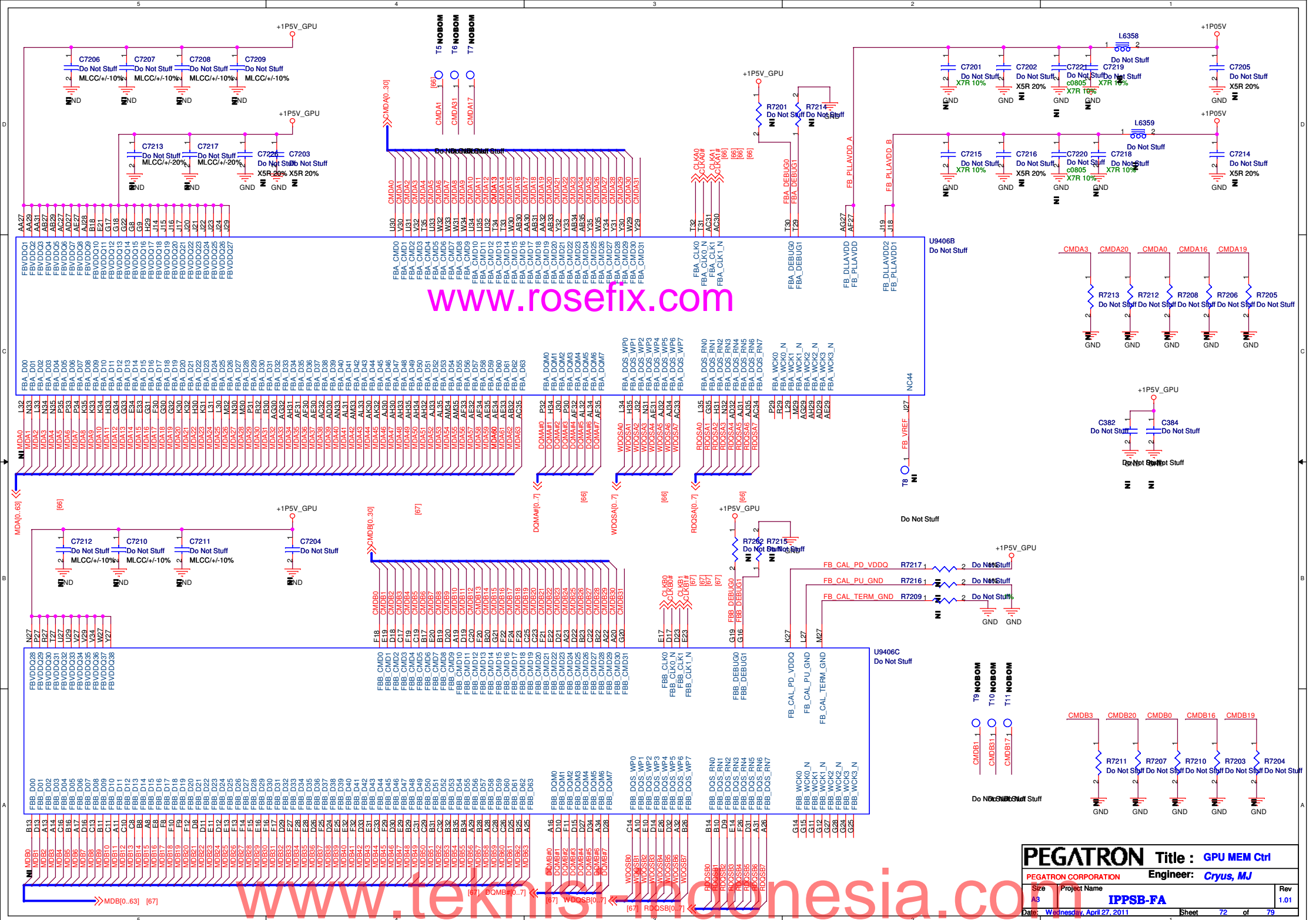
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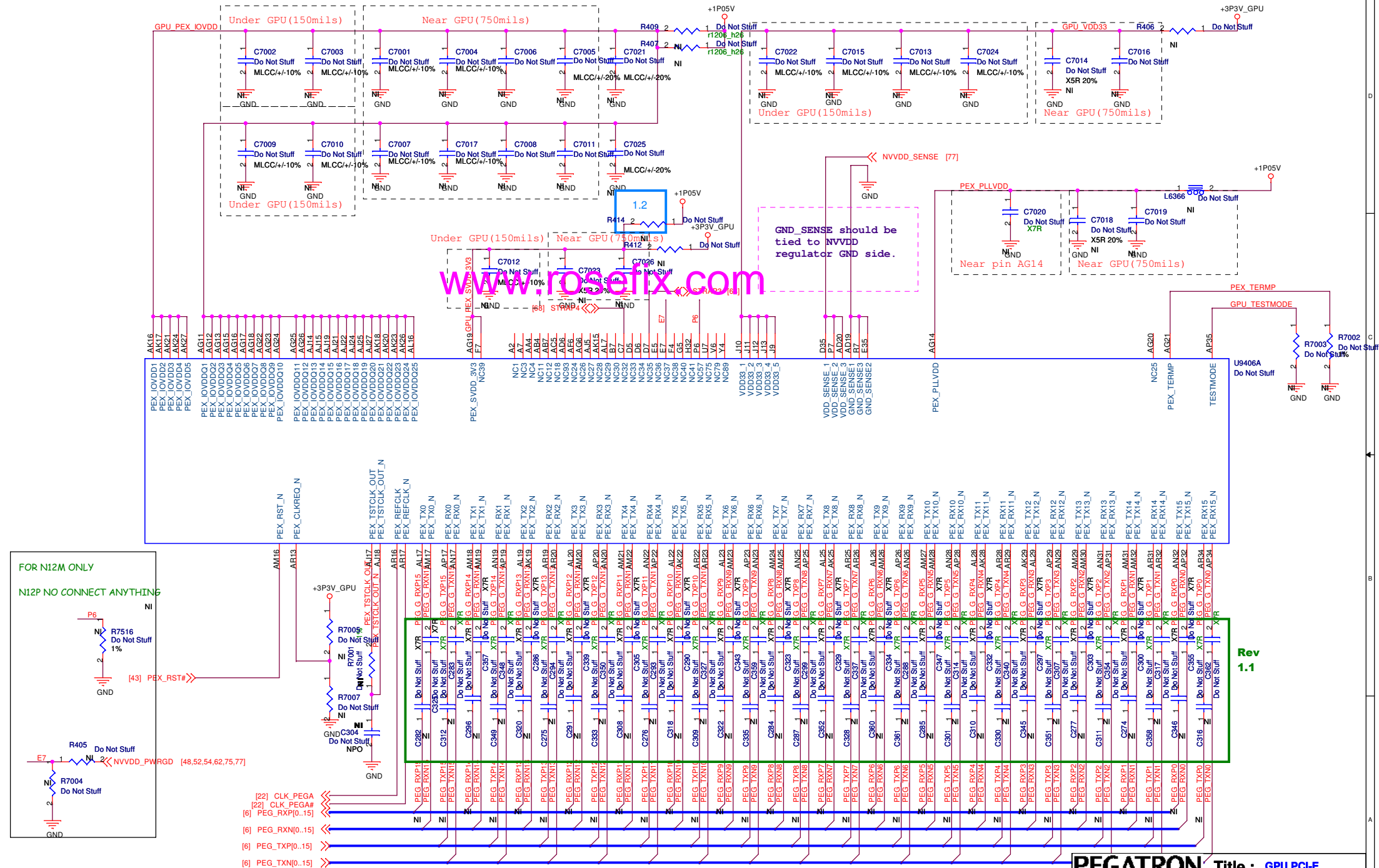
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component

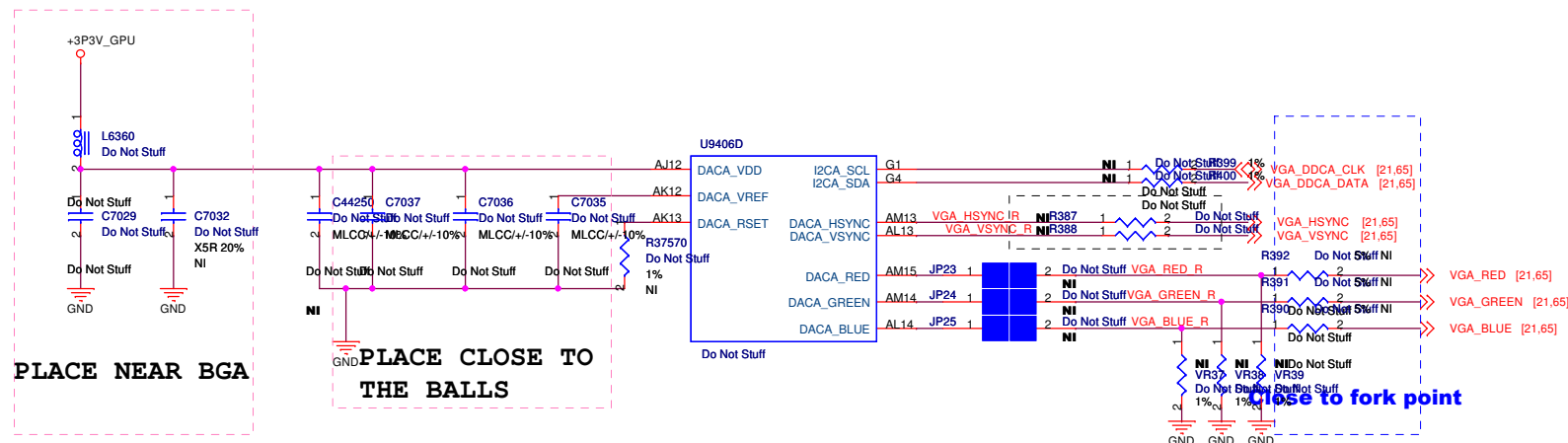
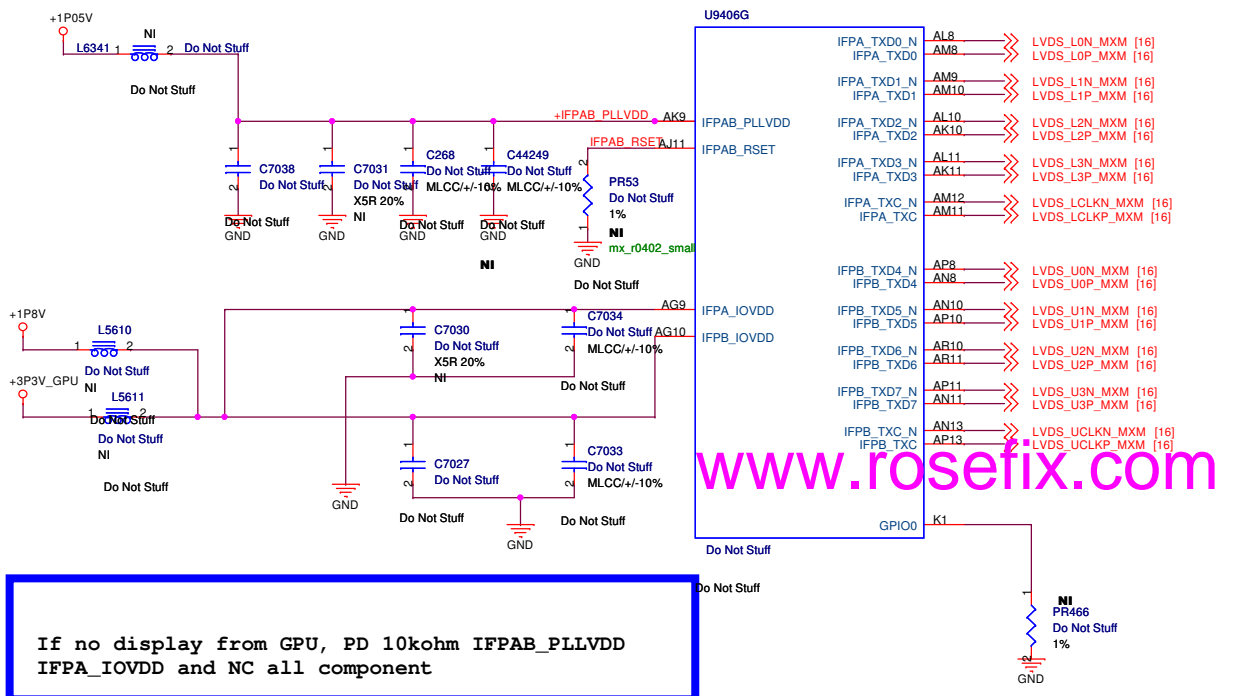


If no display from GPU, PD 10kohm IFPEF_PLLVDD
IFPE_IOVDD and NC all component







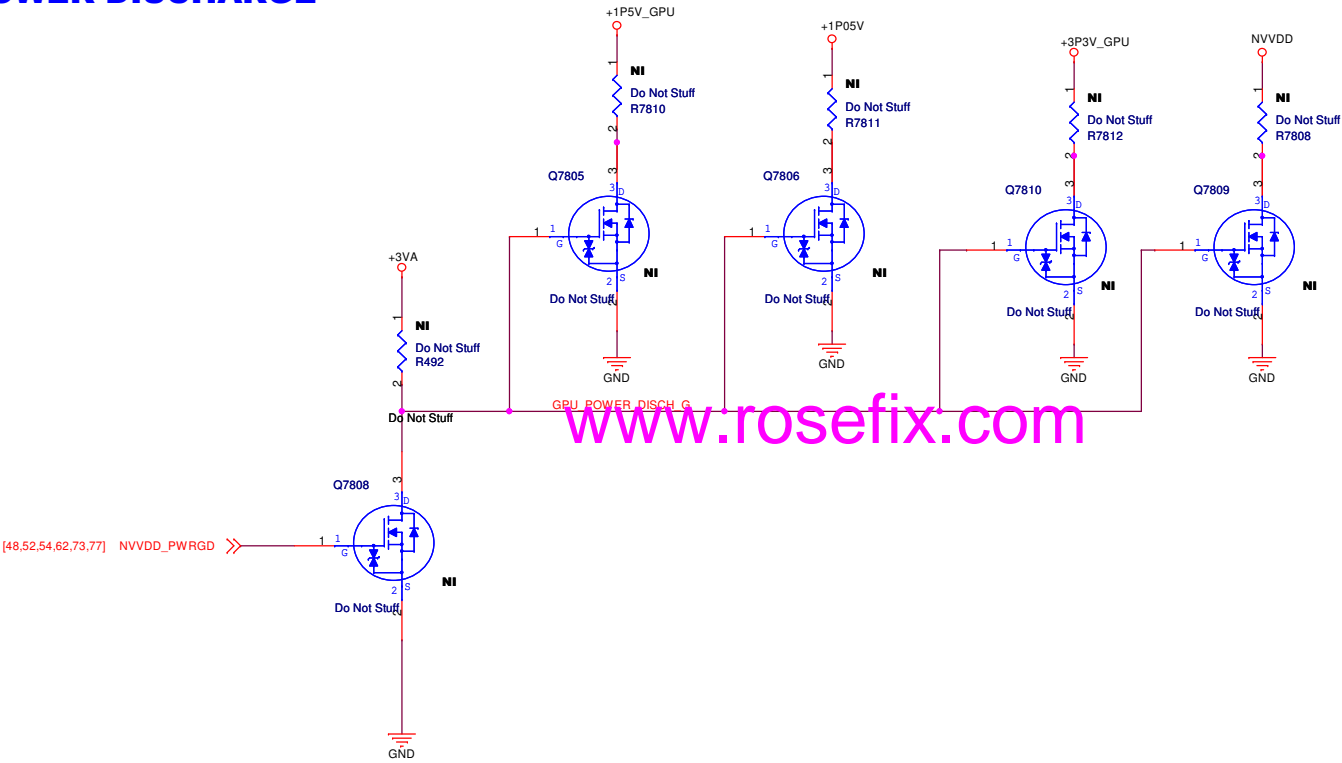


If no display from GPU, PD 10kohm DACA_VDD ,PU 2.2kohm to +3P3V I2CA_SCL I2CA_SDA and NC all component

0413

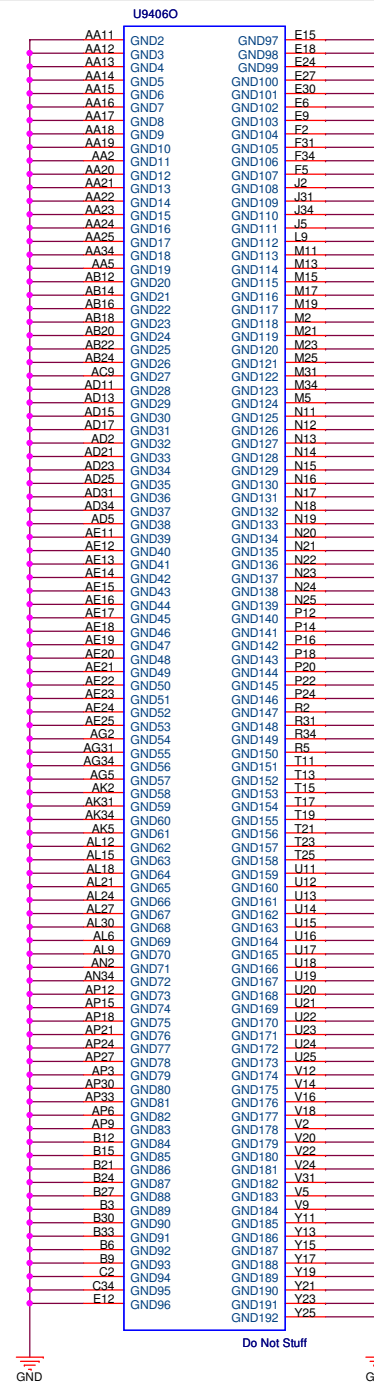
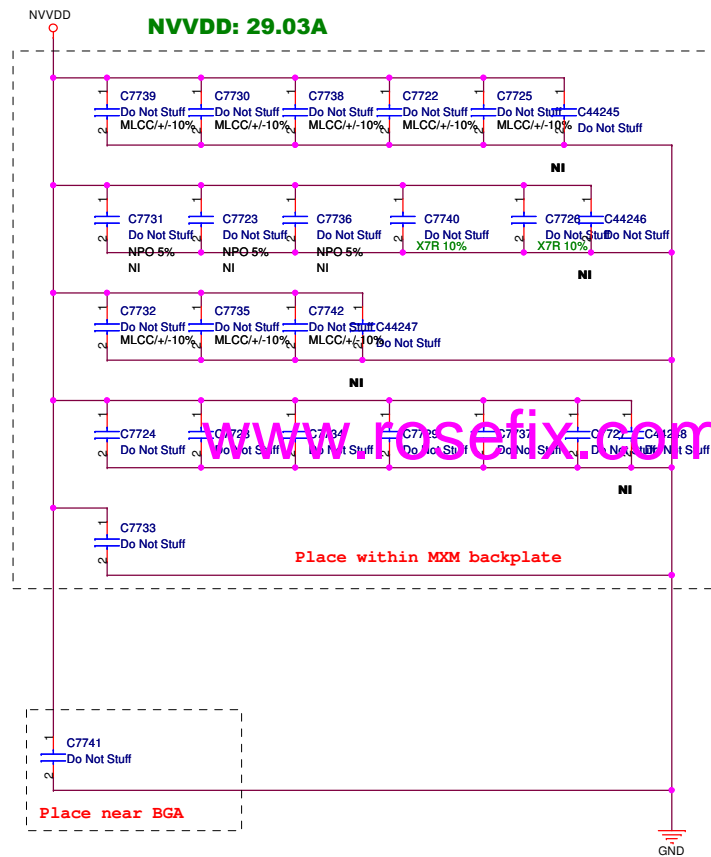
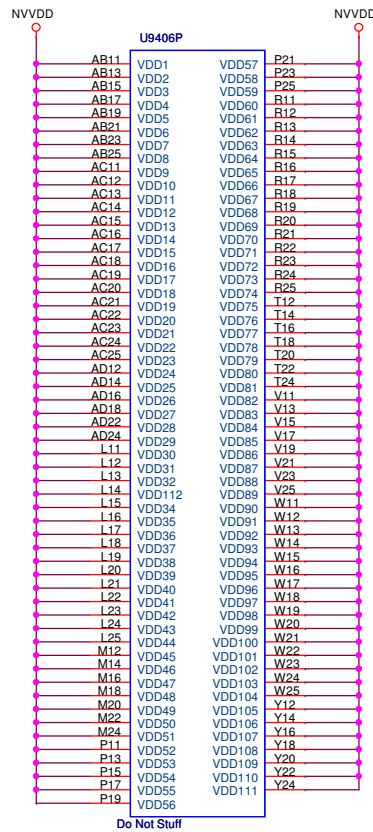
PEGATRON		Title : GPU LVDS VGA	
PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 74 of 79	

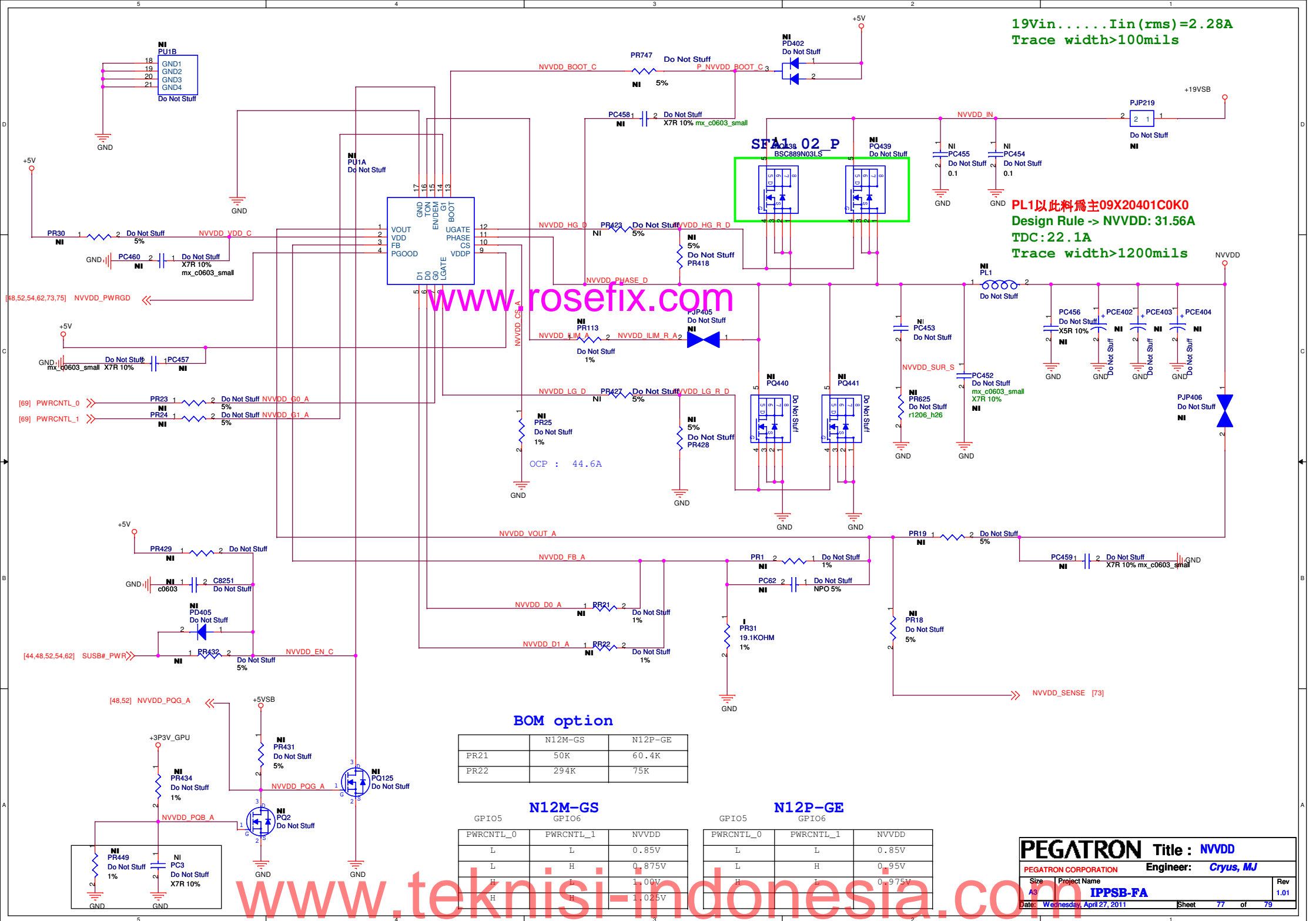
GPU POWER DISCHARGE

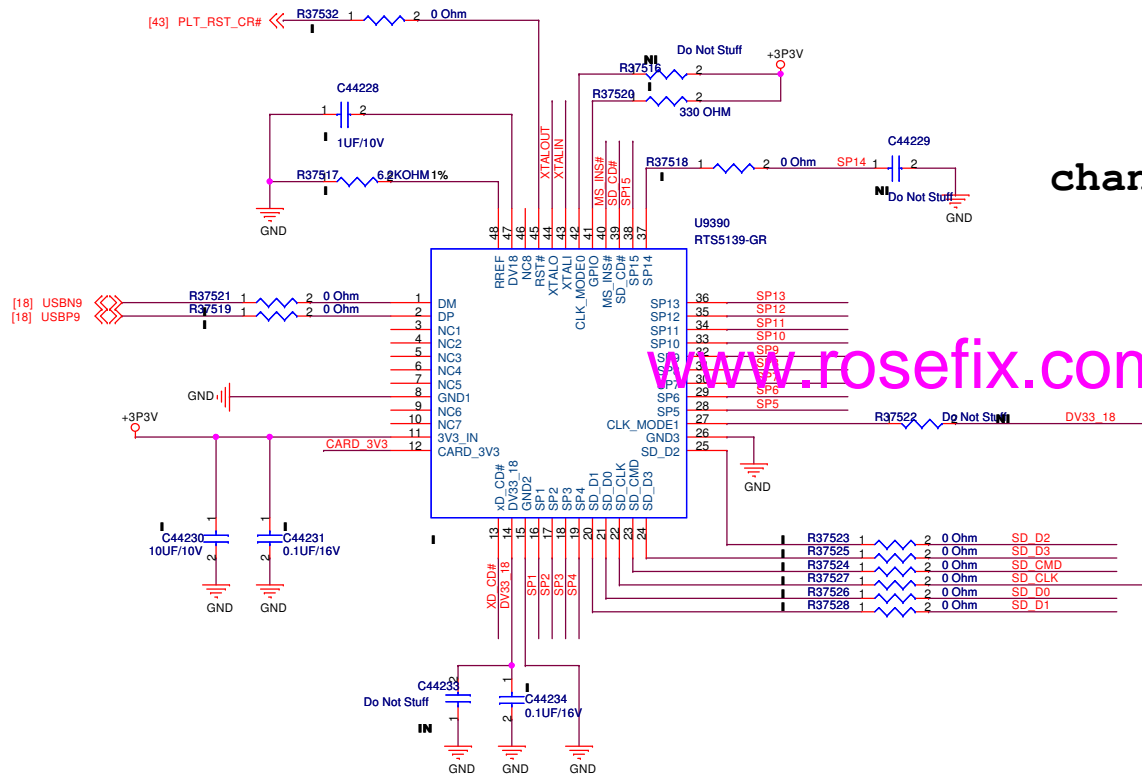


0413		PEGATRON		Title : GPU Discharge
PEGATRON CORPORATION		Engineer: Cryus, MJ		
Size	Project Name	Rev		
A3	IPPSB-FA	1.01		
Date: Wednesday, April 27, 2011	Sheet	75	of	79

12/28 新增
01/07 修改

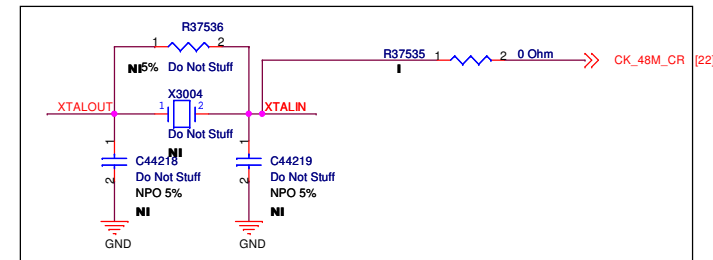






change 48M crystal

SHARE PINGS



SP1	SD D7	XD RDY
SP2	SD D6	XD RE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5		MS BS
SP6		MS D5
SP7		MS D1
SP8		MS D4
SP9		MS D0
SP10		MS D2
SP11		MS D6
SP12		MS D3
SP13		MS D7
SP14		MS CLK
SP15	SD_WP	XD D7

Scott CardReader IO

